OpenROAD v1.0 Expectations

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November 22, 2019

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The OpenROAD v1.0 tool, to be released in July 2020, will be capable of push-button, DRC-clean RTL-to-GDS layout generation in a commercial FinFET process node. The tool is currently visible here. In its v1.0 form, it will be integrated on an incremental substrate provided by the OpenDB database and the OpenSTA static timing engine. It will also offer users and developers Tcl/Python scripting interfaces, and support SoC designs. OpenROAD v1.0 will thus make substantial advances over the “files-based tool chain” seen at the project’s July 2019 "alpha" milestone. At the same time, the functionality of OpenROAD v1.0 will be highly limited relative to that of commercial EDA tools that IC designers are familiar with. Further, the development resources of the OpenROAD project are being largely focused on support of a ~July 2020 SoC tapeout in a commercial FinFET node.

The purpose of this document is to enable future users of OpenROAD v1.0 to have accurate expectations of the tool, and to prepare accordingly to use the tool. This document accepts comments. Please give us your feedback and suggestions.

Expectations for the OpenROAD v1.0 Release

1. Global Considerations
   a. OpenROAD v1.0 production will be focused on the tapeout mentioned in the above introduction. Features will be implemented in priority order based on our sponsor requirement to make the chosen design manufacturable. In Phase 2 of the IDEA program, the OpenROAD tool feature set will be rounded out and more of the project’s flow and tool research objectives will be addressed.
   b. Each new design enablement (foundry process/PDK, library, IPs) will require setup via configuration files, one-time characterizations, etc. as documented with the tool. Examples include (i) the setup of PDN generation, (ii) the creation of “wrapped LEF abstracts” for cells and/or macros to comply with Generic Node Support (see Routing, below), and (iii) the creation of characterized lookup tables to guide CTS buffering.

2. Supported Platforms
   a. OpenROAD v1.0 will build on “bare metal”, CentOS 7 with required packages installed as specified in the README.
b. MacOS will also be supported.

c. Users with access to Docker will also be able to build on any machine using the included Dockerfile.

3. Design Partitioning and Logic Synthesis
a. Logic Synthesis (Brown-Yosys) will accept only hierarchical RTL Verilog.

b. SystemVerilog to Verilog conversion must be performed by the user (e.g., using bsg sv2v or any tool of their choosing) before running Brown-Yosys.

c. Logic Synthesis is one of potentially multiple steps in OpenROAD that may require a single merged LEF as of the v1.0 release. A utility script to perform merging is here.

d. To support convergence in the downstream place-CTS-route steps, it is advisable to exclude cells that risk difficult pin access (e.g., sub-X1 sizes) and/or to invoke cell padding during placement. The cell exclusion would be akin to a “dont_use” list, which is not currently supported and must be manually implemented by editing the library files.

4. STA
a. Supports multi-corner analysis (e.g., setup and hold), but with limit of one mode.

b. SDC support up to latest public, open version (e.g., SDC 1.4).

c. No SI analysis: any coupling caps can be multiplied by a “Miller Coupling Factor” (MCF) and then treated as grounded.

d. No CCS/ECSM (current-source model) support.

e. No LVF support.

f. No PBA analysis option. Only GBA will

g. No instance IR drop (i.e., setting a rail voltage for given instance).

h. No reduction of non-tree wiring topologies. (Arnoldi reduction provided along with O’Brien-Savarino, 2-pole, Elmore reduction and delay calculation options.)

5. Floorplan
a. Macro placement is limited to 100 RAMs/macros per P&R block.

b. PDN configuration files must be provided by the user. These are documented in the “pdn” tool repo, here.

6. Placement
a. A P&R block is limited to one logic power domain and one I/O power domain. Additional power domains must be handled manually (OpenROAD Tcl scripting).

b. Isolation cells, level converters and power management must be manually inserted into the layout by the user (e.g., as pre-placements).

c. No support of UPF/CPF formats for power intent.

d. Support of user guidance for logic clustering and placement will be limited to “fence” and “pre-placement” guidance, with the caveat that such guidance may degrade solution QOR in the OpenROAD flow.

7. Clock Tree Synthesis
a. Support only positive edge-triggered FFs

b. Hold buffering will be at post-CTS and not later in the flow

8. Routing
a. DRC-clean routing is as evaluated by a P&R tool such as Innovus
b. The TritonRoute router will not understand LEF57, LEF58 constructs in techlef: the workaround is OpenROAD Generic Node Enablement (see “OpenROAD Requirements for Generic Node Support”, at this link).
c. Users should be advised that TritonRoute does not handle coloring explicitly; a color-correct-by-construction methodology (e.g., for Mx layers in 14/12nm) is achieved via Generic Node Enablement.
d. Antenna checking and fixing capability is not committed for v1.0.

9. Layout Finishing and Final Verifications
   a. Parasitic extraction (SPEF from layout) is unlikely to comprehend coupling.
   b. There is no “signoff-quality electrical/performance analysis” counterpart to “PrimeTime-SI” (timing, signal integrity) or “Voltus”/“RedHawk” (power integrity).
   c. DRC checking is limited to the equivalent to what a commercial P&R tool would perform after detailed routing.
   d. Generation of merged GDS currently requires a Magic 8.2 tech file. Details are given here.
   e. Export of merged GDS does not add text markings that may be expected by commercial physical verification tools.
   f. For supported design tape-outs (particularly, at a commercial 14/12nm node, up through July 2020), physical verification (DRC/LVS) is expected to be performed by the design team using commercial tools. (Everything up to routed DEF and merged GDS will be produced by OpenROAD or other open-source tools.)
   g. For supported design tape-outs (particularly, at a commercial 14/12nm node, up through July 2020), FEOL/OD/BEOL fill is likely to be performed by commercial tools in the normal physical verification (e.g., Mentor Graphics Calibre) flow. Should this be the case, FEOL/OD/BEOL fill synthesis will not be committed for OpenROAD v1.0 in July 2020.