MALENDA 2018
Closing Panel

Paul Franzon, NCSU
Rajeev Jain, Qualcomm
Brucek Khailany, NVIDIA

Andrew B. Kahng, UCSD (moderator)

Two Driving Questions

- **What does ML in EDA require in future open-source Tools + Benchmarks + Data ?**
- **What EDA flows offer the best / worst "bang for the buck" for ML ?**

- **Paul Franzon:** Distinguished Professor and Director of Graduate Programs in ECE at NOrth Carolina State University. He is also the NCSU site Director for the NSF/Industry Center for Advanced Electronics though Machine Learning.
- **Rajeev Jain:** Professor Emeritus at UCLA and Technology Lead at Qualcomm. He was elected Fellow of the IEEE for his contributions to Computer-Aided Design. His recent interest is in applying machine learning to optimize designs for complex SOCs in deep submicron processes.
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NC STATE UNIVERSITY

CAEML
CENTER FOR ADVANCED ELECTRONICS THROUGH MACHINE LEARNING

Tools and Benchmarks

Paul Franzon,
Cirrus Logic Distinguished Professor,
Director of Graduate Programs,
Site Director, CAEML,
Department of Electrical and Computer Engineering,
NC State University

Georgia Tech

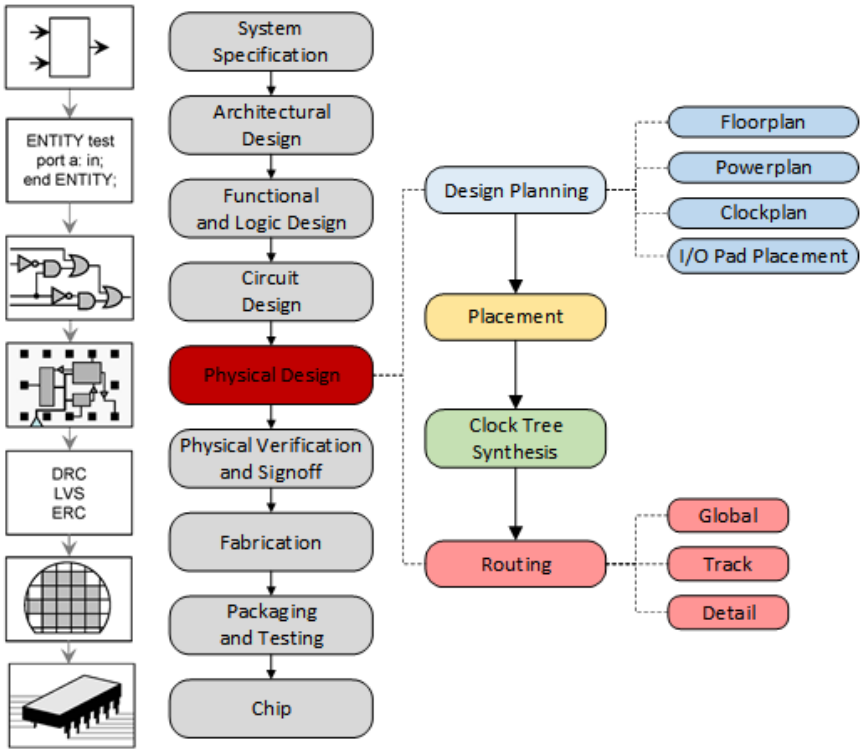
ILLINOIS
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

NC STATE UNIVERSITY

NSF

Data Collection is Hard

- Example of data collection:
- Project 2A7: Automated back end design



After a lot of scripting by PhD students

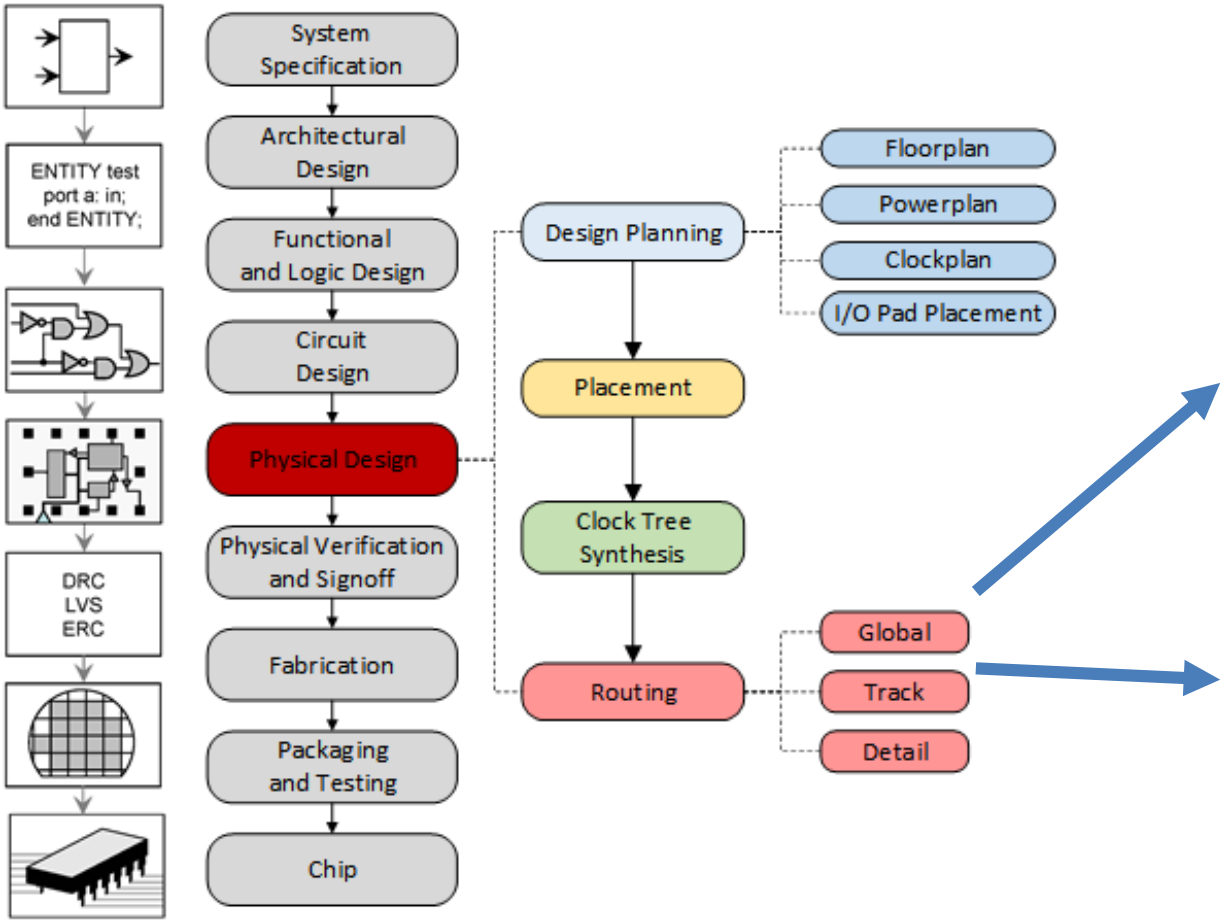
- Collection of models used to drive design:

		Cell Area		Critical Path Length	
		CA (μm^2)		**CPL** (ns)	
Design	**Collection Time**	**Min**	**Max**	**Min**	**Max**
AES	7.26 Hours	22190	49780	1.85	5.55
CORTEX	5.94 Hours	11950	26000	2.82	14.60
CSA	31.00 Minutes	570	1465	0.51	3.4
FSM	39.00 Minutes	170	443	0.60	1.26
XBAR	21.32 Hours	7586	21301	0.94	2.93

EDA flows should be instrumented

- Every design run through the team should have key data automatically extracted
- Cant just be data dump of layouts though
  - Data explosion
- Challenge is working out what key and enabling data to collect

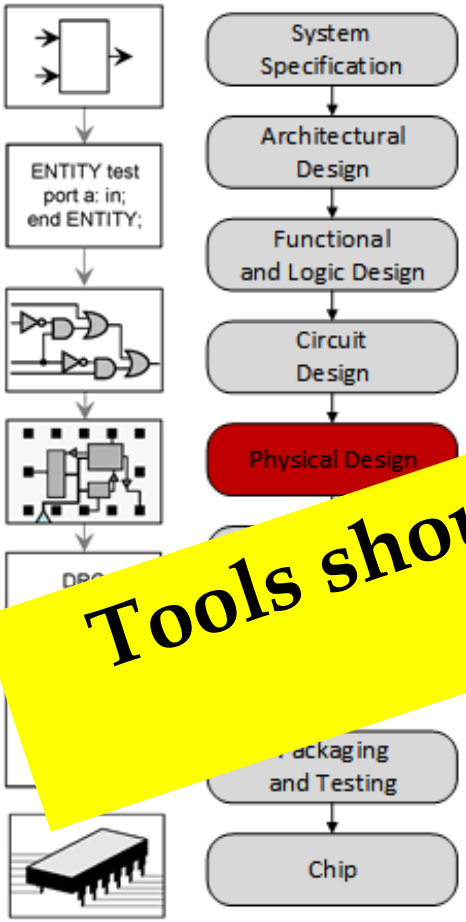
Example: Global Routing



Tool settings

Congestion Map
Timing
Area, etc.

Example: Global Routing



System Specification
Architectural Design
Functional and Logic Design
Circuit Design
Physical Design
ackaging and Testing
Chip

Design Planning
Floorplan
Powerplan
Clockplan
I/O
Placeme
Routing
Global
Track
Detail

Tools should come instrumented and not rely on user scripting.

Congestion Map
Timing
Area, etc.

Benchmarks

- Its very hard to get useful design data from companies
- We recently got a dump of designs from a large company
  - Many of the designs clearly did not work
- What is needed is a corpus of quality, verified large designs that can exist in the public domain
- Universities must play a leading role in generating and collecting thus
- Just like the NCSU PDKs and Nangate cell library

Which Tools Should be Instrumented?

- All flows in which input setting alternatives affect quality of the results
  - Usually requiring multiple human experiments
  - E.g. Back end design
- All tools interacting with the fab
  - DFM, DFT, etc.
- For the future:
  - Tools that rely heavily on designer expertise

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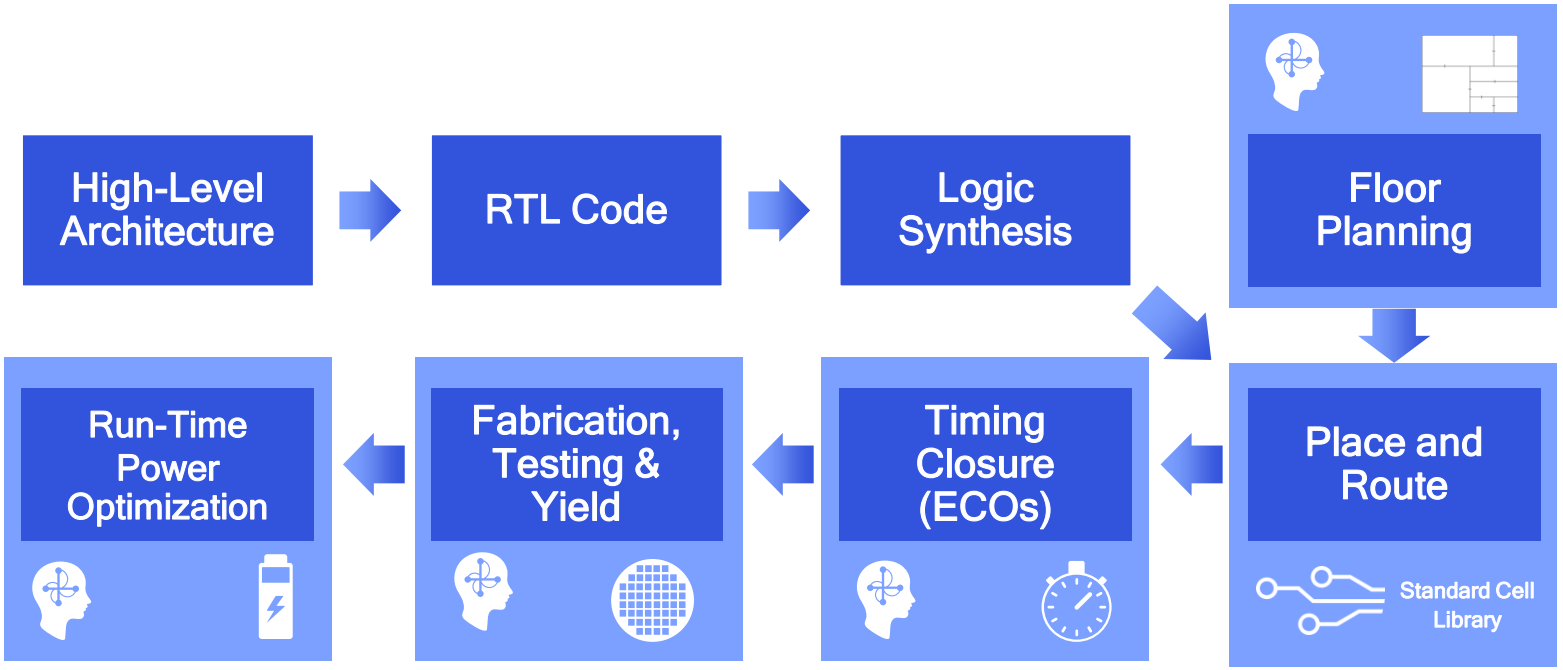
SoC Design Process: Gaps in Automation

Human in the loop needed to fully meet design targets

Qualcomm



TUESDAY June 26, 1:30pm - 3:00pm | Room 3024, SESSION 24 The Road to No-human-in-the-Loop Design

➢ **24.2 Efficient Reinforcement Learning for Automating Human Decision-Making in SoC Design**

Shankar Sadasivam - Qualcomm Technologies, Inc., San Diego, CA

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DAC WORKSHOP: MACHINE LEARNING IN DESIGN AUTOMATION (MALENDA)

Brucek Khailany, Director of ASIC & VLSI Research, NVIDIA

Acknowledgement: Mark Ren, Senior Research Scientist, NVIDIA

June 24, 2018

REQUIREMENTS FOR OPEN-SOURCE ML IN EDA

Data

- **Challenges:** Quantity & quality of data; IP sharing issues; lack of public datasets; Data extraction and feature representation.
- **Potential Solutions:** Academic communities can take the lead on open-source datasets; Leverage open-source designs (RISC-V, NVDLA), Use transfer learning for private data.

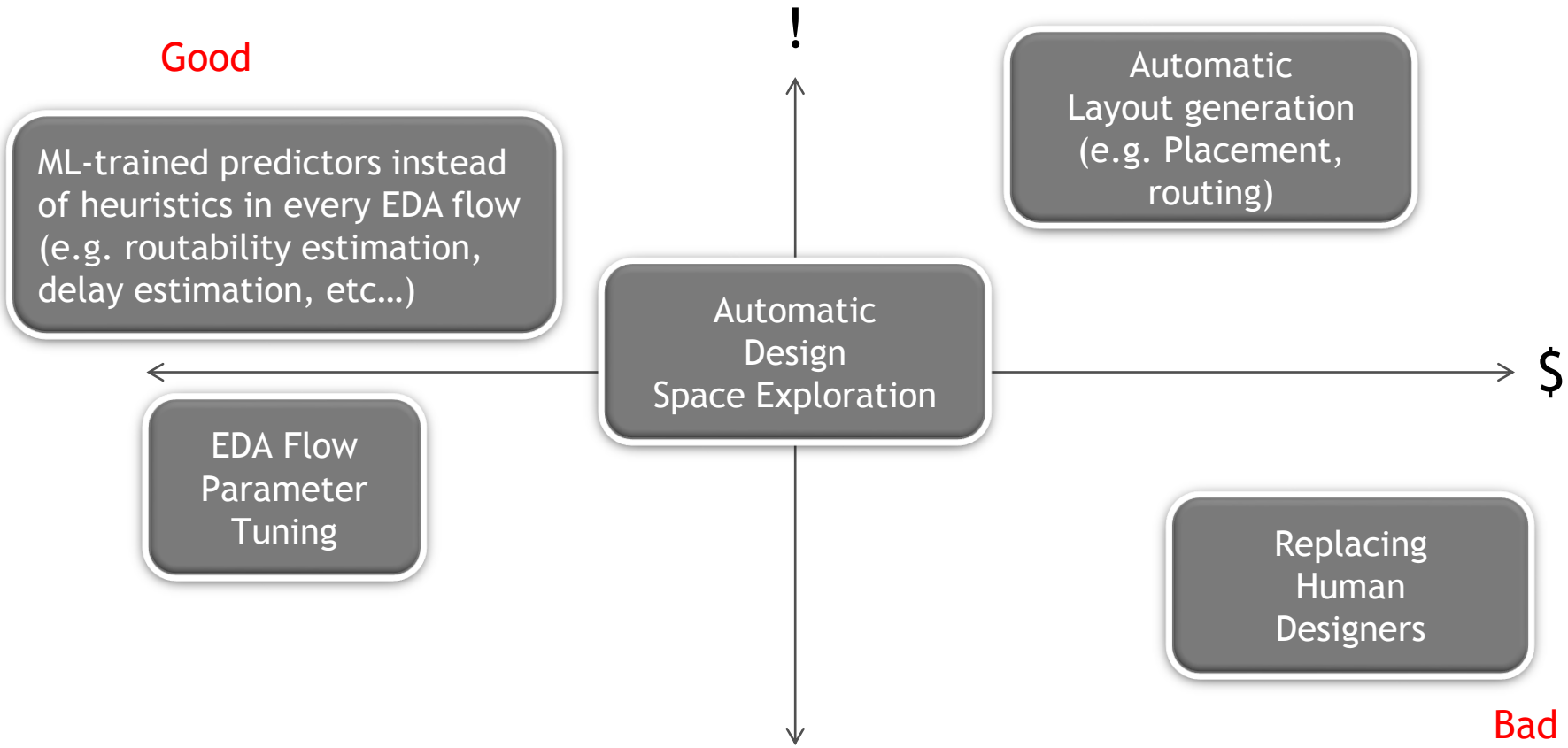
Tools

- **Challenges:** Lots of compute needed for training, Interoperability with commercial tools; Infrastructure for connecting EDA formats with python-based ML frameworks.
- **Potential Solutions:** Leverage cloud resources for DL training;
  Develop open-source packages for connecting EDA formats with ML frameworks.

Benchmarks

- **Challenges:** RTL->GDSII is a complicated multi-step process; Different companies have different benchmark objectives.
- **Potential Solutions:** Break complex flows into multiple separate benchmarks; Develop competitions for solving specific EDA-related problems with a standard dataset (similar to ImageNet).

!/$ OF USING ML FOR EDA FLOWS



NVIDIA

Panel Question Inputs 1/2

- (1) Having access to right quantities of relevant and current data (with high BW access) is key, especially to optimize flows. **How have you organized your data inside your companies to effectively drive ML for design flows? (2) Being able to generate lots of data points is limited by access to #licenses to relevant EDA software. How do you deal with this surge in need?**
- **What are the hardware compute setup needs for EDA ML applications?**
- Some percentage of data is used for training and some is used for testing. How do one choose the training and test set to guarantee repeatability?
- Q: What will be the business impact (if any) of ML applications in EDA flows and tools? Will there be any visible change in the classical SW licensing models? And if so in what timeframe?
- **ML algorithm based optimization (design, testing, manufacturing) should always be validated by deterministic verification methods. Do you see a possibility that ML optimization methods become too complex, and no corresponding deterministic verification methods can be found. What will be the solution - not using the ML based optimization, or using it without validation?** Example: ML based generation of test cases vs. Metric to measure completeness of testing.
- Can we see ML adoption go beyond EDA space, such as in Process Control? If yes, what could be the first applications?

Panel Question Inputs 2/2

- **Khailany/Jain: what ML practices have they already started exploring?**
- **How can industry help with providing high quality, anonymized data set for ML? Who should own driving this effort.**
- **What instances/applications of ML are being actively used by major EDA companies and design companies?**
- 1. how hard it would be to debug if there is any problem in the training, model, inference? 2. do design engineers (especially those working on ASIC logic synthesis, sta, pnr) have to know lot of the underlying math to enable the usage of ML in their day to day work in future?
- Where do you see applications of machine learning for analog centered eda?
- **What are the pain points in the current design and manufacturing flows that you have no good Eda solution that you look towards Machine learning to solve?**
- **Given that ML depends on data, both positive and negative results, how realistic is it for EDA practitioners to generate usefully large data sets given how expensive this can be for hardware related tasks? Lots of start ups and even well established companies are touting ML-based technologies as though they are some sort of magic wand, but they are often experts in either Design Automation *or* ML, rarely both. What examples of new technologies have you seen that look like they will genuinely be disruptive?**
- New data may be needed for different designs and technologies. This can be a complex training problem. Thoughts?

Mining the Panel Question Inputs …..

- **TODAY: What are the hardware compute setup needs for EDA ML applications?**
- **Khailany/Jain: what ML practices have they already started exploring?**
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- **How can industry help with providing high quality, anonymized data set for ML? Who should own driving this effort.**
- **PAIN: What are the pain points in the current design and manufacturing flows that you have no good EDA solution that you look towards Machine learning to solve?**
- **DATA+LICENSES+…**(1) Having access to right quantities of relevant and current data (with high BW access) is key, especially to optimize flows. **How have you organized your data inside your companies to effectively drive ML for design flows? (2) Being able to generate lots of data points is limited by access to #licenses to relevant EDA software. How do you deal with this surge in need?**
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- **ANALOG: Where do you see applications of ML for analog centered EDA?**