DARPA is building a silicon compiler

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We are losing the complexity battle

Sources: Economist, IBIS

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DARPA’s $100M Hardware Compiler Investment

No human in the loop mixed signal circuit layout

No human in the loop package and board layout

Intent driven design and system synthesis

A viable open source hardware design ecosystem

Image Source: Raspberry Pi
End State – The first general purpose Silicon Compiler

$ git clone https://github.com/darpa/idea
$ git clone https://github.com/darpa/posh
$ cd posh
$ make soc42

Image Sources: Amazon, NVIDIA

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What it takes to build a hardware compiler

IDEA Program
11 Teams
16 Subcontractors
26 Professors
35+ Professionals
60 Graduate Students

POSH Program
11 Teams
10 Subcontractors
18 Professors
35+ Professionals
39 Graduate Students

22 Teams Across 17 States

57% Academic Institutions
43% Industry

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Sample of Program Research Efforts

Cadence Design Systems
Analog Layout

University of Washington
Open source analog IP

JITX/NGMS
Design by intent

Yale
Asynchronous Design

University of California at San Diego
Digital Layout

Synopsys
Mixed Signal Emulation

University of Washington
RISC-V

Xilinx
Mixed HW/SW Emulation

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IDEA: A unified electrical circuit layout generator

**Today**

- Knowledge embedded in humans
- Limited knowledge reuse
- Reliance on scarce resources

- Chip: 9 months
- Package: 3 months
- Board: 3 months

**Future**

- Knowledge embedded in software
- 100% automated hardware compilation
- 24 hour turnaround

- Data
- Training
- Models

- IDEA Unified Layout Generator

- Chip
- Package
- Board

24 hours

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**IDEA:** No human in the loop digital AND analog layout!

### Today
Designer provides manual constraints to layout person (or tool)

- **Max 10µm from main supply, 0.5µm width**
- **Common centroid layout**
- **Place dummies, interdigitize**

### Future
Automatically assign constraints based on trained circuit & layout models

- **Millions of circuits**
  - Training
  - Circuit Classifier
  - Assign Strategies & Constraints
  - Auto-placement
  - Auto-routing

**Centroid Mirroring Isolation**

**Common Vocabulary of Strategies**
- Centroid
- Mirroring
- Isolation

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IDEA: Intent-driven system synthesis

**Intent**: Specify what, not how!
Most true board specifications should be very minimal.

**True Specs:**
- 5V
- Ethernet
- USB
- HDMI
- 1GB RAM
- 128MB Flash
- FPGPA
- 20 GFLOPS
- ARM A9

**Derived**: 500 Parts, voltage levels, placement, routing, connectivity
IDEA: An open 5M+ component IC database

Today

- 5M+ parts in circulation
- Information embedded in datasheets and reference designs
- No standard models
- Automatic optimization not possible

IDEA

- IC standard models (LEF,LIB,IP-XACT)
- Extend standards for boards / SIPs
- Creation of 5M+ part DB
- Model all properties needed for constraint-based system optimization

Source: data sheets from Xilinx, Analog Devices

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DARPA  POSH: Expected Program Results

RI SC-V

Multicore RI SC-V

Open source FPGA Chips

“Linux for SoC Design”

Open source analog IP

Signoff level validation

Commercial open source design community

Image sources: Farhek, Wikipedia, EE Times

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Silicon Compiler Program Schedule

2018
- Program Kickoff

2018
- First Integration Exercise

2019
- Alpha Release, working code

2020
- Working Beta Silicon Compiler
  - 50% PPA

2022
- Program Completion
  - 100% PPA

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Image Source: Raspberry Pi
Money

Semiconductor disruption enabled by IDEA and POSH
<table>
<thead>
<tr>
<th>Time</th>
<th>Distance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ns</td>
<td>Foot</td>
</tr>
<tr>
<td>1 us</td>
<td>Eiffel Tower</td>
</tr>
<tr>
<td>1 ms</td>
<td>NY to Boston</td>
</tr>
</tbody>
</table>
Gravity

Real time machine learning?

Image Sources: Drone Air, IBM
Space

• Original Intel 4004
• 2,300 transistors
• Fits in a cell at 3nm?

Image Sources: Intel, CGTrader

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“Since my 1965 paper that ERI references, what has actually happened in the intervening 52 years is far beyond anything I contemplated. It is a testimony to the creativity of many engineers and scientists that the industry has surmounted apparent roadblocks that looked to be the end of transistor scaling.”

- Gordon Moore, December 1, 2017

Electronics Resurgence Initiative Summit

San Francisco, CA
Palace of Fine Arts
July 23-25, 2018
www.ERI-Summit.com

What to Expect

- Hear from leading voices in the microelectronics industry
- Engage directly with DARPA’s thought leaders and a network of experts
- “What’s Next” Technical Brainstorming Workshops: Hardware Emulation, Integrated Photonics, Hardware Security, and Hardware for Next Gen Artificial Intelligence

Hear from Leading Voices

John Hennessy
Chairman, Alphabet

Gary Dickerson
CEO, Applied Materials

Aart de Geus
Co-CEO, Synopsys

Walden Rhines
CEO, Mentor

Tom Beckley
Senior VP, Cadence

Mike Mayberry
CTO, Intel

Bill Dally
SVP, NVIDIA

Erica Fuchs
Professor, CMU

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