SOC Design Roadmap Activities in Japan

Low Power Design Technique for SOC

<Challenges and Solutions>
~Toward keep consistent with design productivity improvement~

JEITA (Japan Electronics and Information Technology Association)
STRJ (Semiconductor Technology Roadmap committee of Japan)
WG1 (Design Technology Working Group)

2010 June 14
STRJ Committee Structure

JEITA Semiconductor Board (JEITA-JSIA)

Semiconductor Technology Committee

Semiconductor Technology Roadmap committee of Japan (STRJ)

Number of members: 7 companies
Chairperson: Hidemi Ishiuchi, Toshiba Corporation

Activities:
The Semiconductor Technology Roadmap Committee of Japan predicts technological advancement by item in semiconductors for next 15 years, cooperating with International Technology Roadmap for Semiconductors - ITRS.
How STRJ works with ITRS

ITRS

Introduction

Grand Challenges

ORTC
Overall Roadmap Technology Characteristics

Each Technology

Define LSI products which drive manufacturing and design technology

Roadmap of Design Technology

System Drivers

Design

Test and ATE

PIDS

FEP

Asm. and Pkg.


Work in Progress - Do not publish
Mission of Design WG(WG1)

◆ International Activities: In charge of ITRS “System Drivers Chapter” and “Design Chapter”
   – System Drivers Chapter
     • Defines LSI products that drive all the technical field of ITRS
   – Design Chapter
     • Presents future challenges of design technologies with proposed solutions

◆ Domestic Activities:
   – Quantifies SOC structure and size as the presented foundation roadmap deliberation
   – Gives quantitative analysis to design technology challenges (from “design productivity” and “power consumption” perspectives) on time axis, and propose solutions (develop roadmap)

◆ Expected effects
   – Quantify impacts of ITRS roadmap against SOC design and send out that information
   – Triggers review of ITRS roadmap
   – Help acceleration of design technology innovation (to EDA vendors)
### WG1 (Design WG) members (FY2008)

<table>
<thead>
<tr>
<th>Name</th>
<th>Company</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mikio Sumitani</td>
<td>Panasonic</td>
</tr>
<tr>
<td>Masami Matsuzaki</td>
<td>Fujitsu Microelectronics</td>
</tr>
<tr>
<td>Tamotsu Hiwatashi</td>
<td>Toshiba</td>
</tr>
<tr>
<td>Haruhisa Kashiwagi</td>
<td>STARC</td>
</tr>
<tr>
<td>Tadao Toyoda</td>
<td>Sharp</td>
</tr>
<tr>
<td>Katsutoshi Nakayama</td>
<td>Renesas Technology</td>
</tr>
<tr>
<td>Hiroshi Shibuya</td>
<td>NEC Electronics</td>
</tr>
<tr>
<td>Kazuya Morii</td>
<td>Sanyo Semiconductor</td>
</tr>
<tr>
<td>Junichi Karasawa</td>
<td>Seiko Epson</td>
</tr>
<tr>
<td>Masaru Kakimoto</td>
<td>Sony</td>
</tr>
<tr>
<td>Kenshi Asai</td>
<td>Rohm</td>
</tr>
<tr>
<td>Ichiro Yamamoto</td>
<td>Rohm Group (OKI Semiconductor)</td>
</tr>
<tr>
<td>Koichiro Ishibashi</td>
<td>Renesas Technology</td>
</tr>
<tr>
<td>Yoshimi Asada</td>
<td>Fujitsu Microelectronics</td>
</tr>
<tr>
<td>Toshitada Saito</td>
<td>Toshiba</td>
</tr>
<tr>
<td>Hiroki Tomoshige</td>
<td>Panasonic</td>
</tr>
<tr>
<td>Nobuto Ono</td>
<td>JEDAT</td>
</tr>
<tr>
<td>Masaharu Imai</td>
<td>Osaka University</td>
</tr>
</tbody>
</table>
FY2008 Domestic Activities

Activities with the theme: “SOC power consumption”

Concrete Actions

- Revision of Consumer Portable SOC model based on the latest architecture trend
- Calculation of power consumption trend based on new SOC model
- Organize as the roadmap challenges and solutions for low power design technology in contrast with design productivity

[Reference] Activities for Low Power in the past

<table>
<thead>
<tr>
<th>Year</th>
<th>Activity Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2003</td>
<td>Design TF to estimate low power SOC power consumption</td>
</tr>
<tr>
<td>2005</td>
<td>Design WG to estimate Consumer Portable SOC using Design TF estimation equation</td>
</tr>
<tr>
<td>2006</td>
<td>Estimate Consumer Stationary SOC power consumption</td>
</tr>
<tr>
<td>2007</td>
<td>Quantify impact of low power design technology in manufacturing process against design productivity</td>
</tr>
</tbody>
</table>

Work in Progress - Do not publish
What does Low Power Design mean?

Power = \( \frac{1}{2} \cdot \alpha \cdot C_L V_{dd}^2 f \) + \( \alpha \cdot V_{dd} \cdot I_{cell} f \) + \( V_{dd} \cdot I_{leakage} \) + \( V_{dd} \cdot I_{DC} \)

\( \text{Switching power} \)
\( \text{Feed through power} \)
\( \text{Leakage power} \)
\( \text{DC Power} \)

Dynamic Power

Static Power

- Reduction of power consumption means:
  - \( \alpha \): Activation Rate
  - \( C_L \): Load Capacitance
  - \( V_{dd} \): Supply Voltage
  - \( f \): Operating Frequency
  - \( I_{cell} \): Feed through current in a cell
  - \( I_{leakage} \): Leak current
  - \( I_{DC} \): Steady Current

- To be more specific ...
  - To reduce Dynamic Power,
    - reduce load capacity, turn down signals’ amplitude, turn down operating voltage,
    - turn down activation rate, turn down operating frequency
  - To reduce Static Power,
    - set Vth higher, turn down operating voltage, shut down power supply

\[ \text{Reduction of unnecessary activities} \]
\[ \text{Slow down fast-beyond-necessity areas} \]
Not Sacrificing Design Productivity is MUST

To close the gap against required power goal, *multiple* low power design techniques need to be fully used together.

To reduce power...
- reduce load capacitance
- minimize signal amplitude
- turn down activity ratio
- raise Vth
- lower operating voltage
- slow down frequency
- shut off power

**Low Power Design Technique**
- Smaller area, smaller transistors
- Smaller amplitude of memory bit, word
- Clock Gating Technology
- Multiple Vth methodology
- Substrate Bias control
- Multiple Voltage methodology
- DVFS, AVS
- Power Shutoff technology

Low power design gets complicated and negative impact on productivity is increased.

Challenges and solutions of low power design technologies consistent with *design productivities* has been developed as a roadmap.
Low Power Design Technique(1) : Clock Gating

- **Design Technology Overview**
  - Technology of clock feeding stoppage for non-operating circuit
  - Local clock gating – clock feeding stoppage to registers of which inputs are prospectively known to be stable
  - Global clock gating – clock feeding stoppage to inactive blocks

- **Advantageous Effects**
  - Reduction of switching power in operating conditions

- **Design Complexity**
  - Additional circuit required such as latches for preventing glitch propagation or DFT aware
  - How to best gate clocks
  - How to improve fault detection rate for clock gating circuit
  - ... etc

---

**Example of Power Reduction by Gated Clock**

Reduced to 1/5!

Gated Clock

# of cell: 1.1M

---

*Work in Progress - Do not publish*
Low Power Design Technique(2) : Substrate bias control

- **Design Technology Overview**
  - Optimize threshold voltage (Vth) by controlling substrate bias as a function of manufacturing finishing
  - Reduce power consumption based on minimizing current leakage by raising Vth as high as performance allows

- **Advantageous Effects**
  - Reduction of operating leak power

- **Design Complexity (impact on productivity)**
  - Increased complexity with embedding “mechanism of measuring manufacturing finishing and controlling substrate bias” (in case of implementing off chip, then the impact is for test and system design)
  - Cell placement and clock tree synthesis to maximize substrate bias control effects
  - At speed test which is variable critical paths aware based on substrate bias control
  - ..., etc.

Work in Progress - Do not publish
Low Power Design Technique(3): Power Shutoff (Power Gating)

- **Design Technology Overview**
  - Dramatically reduce leakage power by shutting off the power supply to non-operating blocks
  - Embedding power shutoff switches in LSI is called “On-chip Power Gating”
  - One example of power shutting method is “MTCMOS”

- **Advantageous Effects**
  - Reduction of stand-by leakage power

- **Design Complexity (impact on productivity)**
  - Functional Verification for power on/off sequence is required
  - Affirmation of isolator insertion between power islands and connectivity across the boundary is needed
  - Down-hold of rush current is needed
  - Retention circuit needs to be added for saving data
  - ..., etc.

---

Work in Progress - Do not publish

---

[Reference: Hitachi Consulting](http://jp.fujitsu.com/microelectronics/technical/lowpower/)
Design Technology Overview
- Technology of dynamic control over voltage and frequency depending on how heavy the system’s processing load is
- Under the concept of “do the job as slow as possible if you can relax”, if you can get the result with the same clock frequency, you can reduce the power consumption by lowering the operating voltage

Advantageous Effects
- Reduction of operating switching power

Design Complexity (impact on productivity)
- How to make it practical to dynamically control over lowering voltage and slowing frequency without impacting the system operation based on how the system can relax
- Standardization of specification format is needed for communication method and its automation between SOC and Power IC
- Affirmation of level shifter insertion between voltage islands and connectivity across the boundary is needed
- How to make timing verification more efficient which is variable voltage aware and multiple power supply aware (optimization of multiple-corners / multiple-modes)
- ..., etc

出典:マイコミジャーニュアル「ARMプロセッサ活用法 - 低消費電力のための機能「DVFS」「IEM」の仕組み」
Low Power Design Technique (5): **AVS** (Adaptive Voltage Scaling)

- **Design Technology Overview**
  - Technology of best voltage supplying by monitoring SOC operating conditions (process, voltage, temperature, etc)

- **Advantageous Effects**
  - Reduction of operating switching power

- **Design Complexity** *(impact on productivity)*
  - Standardization of specification format is needed for communication method and its automation between SOC and Power IC
  - Affirmation of level shifter insertion between voltage islands and connectivity across the boundary is needed
  - How to make timing verification more efficient which is variable voltage aware and multiple power supply aware (optimization of multiple-corners / multiple-modes)
  - ...., etc

---

1. Power IC
2. Monitor Circuit
3. PMU
4. Power IF

1. Power IC for AVS: Voltage-variable power IC
2. Monitor circuit: Monitors LSI's operating conditions
3. PMU (Power Management Unit): Calculates best voltage condition for LSI and control Power IC
4. Power IF: Tell calculated voltage condition by PMU to Power IC
## Solutions for low power design technologies (1/2)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock Gating (CG)</strong></td>
<td>Clock Tree Synthesis</td>
<td>CTS optimized insertion / Automated CG insertion and RTL equivalency check</td>
<td>Optimization technology for insertion ratio aware automated CG insertion</td>
<td>High Level CG technology / Technology of consolidated design with asynchronous</td>
</tr>
<tr>
<td></td>
<td>Test Design</td>
<td>Improved fault detection ratio for CG inserted circuit</td>
<td>At Speed test technology for CG inserted circuit</td>
<td></td>
</tr>
<tr>
<td><strong>Substrate Bias Control</strong></td>
<td>Efficient processes I/F</td>
<td>Standardization of inner chip spec description, and its chip design technology</td>
<td>Standardization of design and manufacturing I/F (test, board manufacturing)</td>
<td>Standardization of System level description and its system design technology</td>
</tr>
<tr>
<td></td>
<td>Clock Tree Synthesis</td>
<td>CTS technology to minimize clock skew influence</td>
<td></td>
<td>CTS technology at higher level design</td>
</tr>
<tr>
<td></td>
<td>Placement</td>
<td></td>
<td>Auto placement technology to maximize the effects of substrate bias control for each voltage island</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Timing Design</td>
<td>Timing verification technology for multiple voltage design</td>
<td>Accelerated timing verification technology for multiple voltage design</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reduction of signoff corners</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Test Design</td>
<td></td>
<td>Critical paths change aware At Speed test technology</td>
<td></td>
</tr>
<tr>
<td><strong>Power Shut Off</strong></td>
<td>Verification</td>
<td>Power shut off aware functional verification</td>
<td>Optimized Power shut off aware functional verification</td>
<td>Establishment of verification methodology at higher level</td>
</tr>
<tr>
<td></td>
<td>Specification</td>
<td>Standardization of power format</td>
<td>Power Format enhancement</td>
<td>Standardization of higher level power format</td>
</tr>
<tr>
<td></td>
<td>Test Design</td>
<td>Power shut off aware DFT technology</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Solutions for low power design technologies (2/2)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DVFS AVS</td>
<td>Power supply specification</td>
<td>Standardization of specification format of communication method between SOC and Power IC</td>
<td>Advanced communication method and enhancement on specification format</td>
<td>Standardization of format used in high level design</td>
</tr>
<tr>
<td></td>
<td>Power management</td>
<td>Power management technology for variable voltage and multiple power supplies</td>
<td>Advanced power management for variable voltage and multiple power supplies</td>
<td>Power management technology in high level design</td>
</tr>
<tr>
<td></td>
<td>Power Design</td>
<td>Power circuit generation technology allowing variable voltage and multiple power supplies</td>
<td>Advanced power circuit generation technology allowing variable voltage and multiple power supplies</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock Tree Synthesis</td>
<td>CTS technology which minimizes clock skew impact</td>
<td></td>
<td>Clock Tree Synthesis technology used in high level design</td>
</tr>
<tr>
<td></td>
<td>Timing Design</td>
<td>Timing verification for variable voltage and multiple power supplies (Optimization for multi-corners, multi-modes)</td>
<td>Accelerated timing verification and reduced signoff corners for variable voltage and multiple power supplies</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Test Design</td>
<td></td>
<td>DFT Technology for variable voltage and multiple power supplies</td>
<td></td>
</tr>
<tr>
<td></td>
<td>System Design</td>
<td></td>
<td>System aware DVFS</td>
<td>Asynchronous DVFS</td>
</tr>
<tr>
<td></td>
<td>Power Estimate</td>
<td>Accurate estimation of leakage power using power format</td>
<td>Advanced and accurate power estimation in RTL</td>
<td>Advanced and accurate power estimation in high level design</td>
</tr>
</tbody>
</table>
## Potential solutions for productivity improvement for low power design

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Gating</td>
<td>Clock Tree Synthesis</td>
<td>Insertion and formal verification on “RTL”</td>
<td>With considering gating ratio</td>
<td>- System level design</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Mixed with asynch.</td>
</tr>
<tr>
<td>Test design</td>
<td>High fault coverage with clock gating</td>
<td></td>
<td>At-speed test with clock gating</td>
<td></td>
</tr>
<tr>
<td>Power Gating</td>
<td>Verification</td>
<td>Functional verification</td>
<td>Optimized verification</td>
<td>System level verif.</td>
</tr>
<tr>
<td></td>
<td>Power Format</td>
<td>Standardization</td>
<td>Enhancement</td>
<td>System level format</td>
</tr>
<tr>
<td>Test design</td>
<td>DFT with Power Gating</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DVFS/AVS Bias Ctrl</td>
<td>Power management</td>
<td>For variable voltage design</td>
<td>Enhanced technology</td>
<td>System level</td>
</tr>
<tr>
<td></td>
<td>Power routing</td>
<td>Automatic routing for variable voltage design</td>
<td>Enhanced technology</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock tree synthesis</td>
<td>Minimizes the influence of the clock skew</td>
<td></td>
<td>System level</td>
</tr>
<tr>
<td></td>
<td>Timing design</td>
<td>MCMM and STA for variable voltage design</td>
<td>- Shorten TAT</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Reduce signoff corners</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Test design</td>
<td></td>
<td>DFT for variable voltage</td>
<td></td>
</tr>
<tr>
<td>Power Estimation</td>
<td>- High accuracy of leakage power</td>
<td></td>
<td>High accuracy @RTL</td>
<td>High accuracy @System level</td>
</tr>
</tbody>
</table>
### How many EDA Vendors already support today OR will support in the future

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Gating</td>
<td>Clock Tree Synthesis</td>
<td>With considering gating ratio</td>
<td>- System level design</td>
<td>- Mixed with asynch.</td>
</tr>
<tr>
<td></td>
<td>Test design</td>
<td>High fault coverage with clock gating</td>
<td>At-speed test with clock gating</td>
<td>System level verification</td>
</tr>
<tr>
<td>Power Gating</td>
<td>Verification</td>
<td>Optimized verification</td>
<td>System level verification</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Format</td>
<td>Standardization</td>
<td>Enhancement</td>
<td>System level format</td>
</tr>
<tr>
<td></td>
<td>Test design</td>
<td>DFT with Power Gating</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DVFS/AVS Bias Ctrl</td>
<td>Power management</td>
<td>Enhanced technology</td>
<td>System level</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power routing</td>
<td>Enhanced technology</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock tree synthesis</td>
<td>Minimizes the influence of the clock skew</td>
<td>System level</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Timing design</td>
<td>MCMM and STA for variable voltage design</td>
<td>Shorten TAT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Test design</td>
<td>DFT for variable voltage</td>
<td>Reduce signoff corners</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Estimation</td>
<td>- High accuracy of leakage power</td>
<td>High accuracy @RTL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Support power format</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Blue number indicates number of vendors already support today, red number indicates number of vendors who will support in the future. (WG1 made a questionnaire to 7 EDA Vendors)

Work in Progress - Do not publish
Related Web Site URL

• Official home page of ITRS
  – http://public.itrs.net/
  – Not just ITRS 2009, What’s new of ITRS

• Home page of JEITA Roadmap
  – http://strj-jeita.elisasp.net/strj/index.htm
  – Japanese version of ITRS 2007
  – Information of STRJ activities
    (Semiconductor Technology Roadmap expert committee)