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Andrew Kahng on Industry-Academia Cooperation

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At CDNLive Silicon Valley, Professor Andrew Kahng of UCSD gave a presentation titled *Toward New Synergies Between Academic Research and Commercial EDA*. The paper won the best paper award for the academic track.

Andrew started off by pointing out that EDA and academia have some long-standing differences in perspective.

EDA thinks:

- Your students end up working for Google anyway
- We'd like your student to come for the summer and implement her DAC paper (never mind who supported the research)
- We need to see ROI on our $
- Sorry, any testcases would be customer/partner data that we cannot disclose

Meanwhile, academia thinks:

- You depend on us to train your students. We don't get the respect or $ we deserve
- We need $ to be able to work on your problems; we're not your R&D department
- EDA companies don't support research, so students go to other fields
- Sorry, you didn't support that research, so now you'll need to talk to our technology transfer office
- Better benchmarks and data lead to more useful research

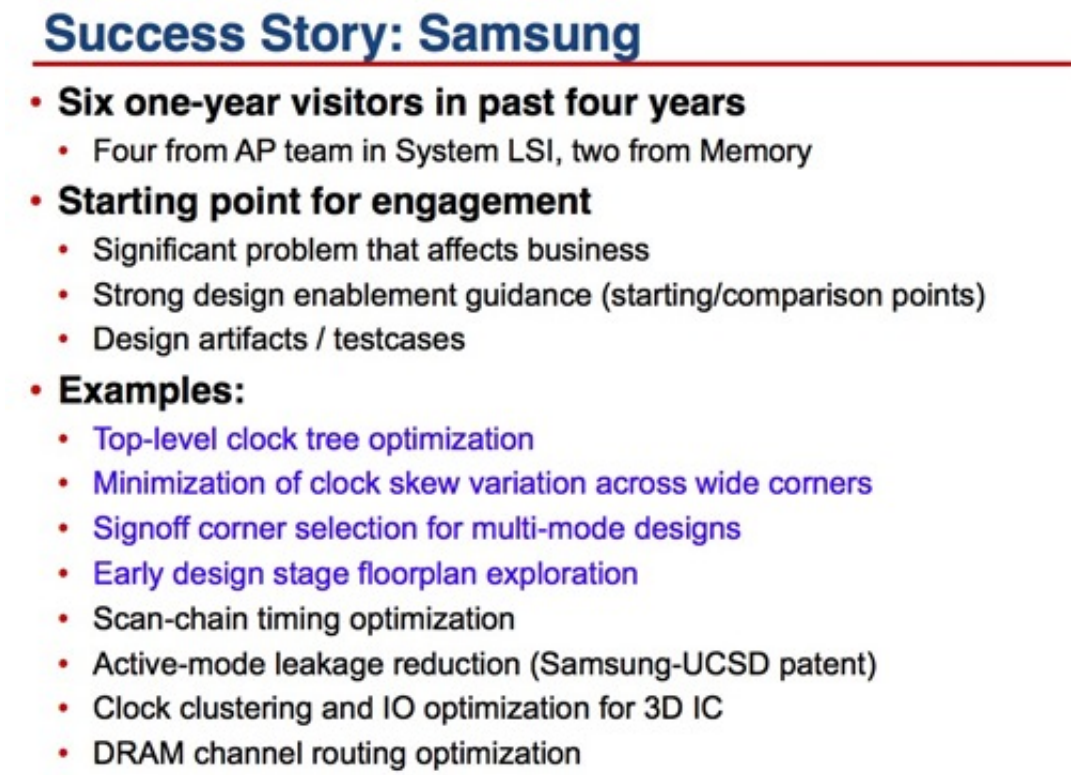
None of this is exactly new. Andrew went back to a panel he'd presented at ICCAD in 2006. He had the actual slides he presented then, just to show how the issues remain similar ten years later.

Here's just one slide:

An interesting aside is that the entire funding of all the projects during his career, which resulted in over 300 papers, lots of patents, 16 PhDs supervised (that was to 2006 so I assume it may be more now) is roughly the same as the series A funding for an EDA startup.

So what do successful projects look like? In the 10 years since 2006, Andrew Kahng and his group have worked closely with Samsung, Qualcomm, NXP, imec, ASML, Broadcom, and other companies that are on the cutting edge of design and manufacturing in the most advanced processes. One notable omission: there are no EDA companies on the list.

The experience with Samsung has been positive:



For example, one published work on clock tree optimization led to a reduction of 51% in the wirelength of the top-level

tree, and a reduction of 320ps in worst-negative-slack (WNS). There were half a dozen other successful joint projects that resulted in impressive results. It is worth emphasizing that these are real-world projects and the results impact production silicon. Although done in academia, these are not academic exercises in the usual sense of the word.

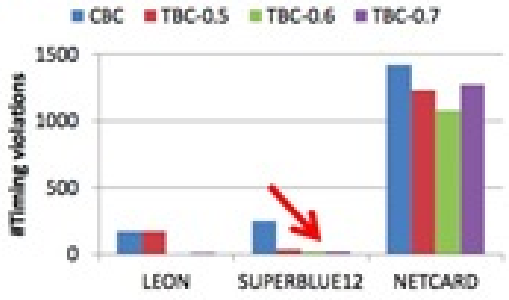
Another successful partnership was with Qualcomm:

Success Story: Qualcomm

- **Engagement across research, advanced tech, VLSI tech**
- **Starting point for engagement**
  - Problem formulations in signoff, margin reduction arena
  - Design rule / signoff corner information
  - Calibration of modeling assumptions (e.g., PLL jitter, flop trays, netlist statistics,)
  - Lots of F2F meetings, Starbucks meetings
- **Topics include**
  - Tightened BEOL corners
  - Flexible FF timing model
  - Mixed-height placement
  - Process-aware voltage scaling (on-die monitors)
  - Minimum implant area aware sizing and placement

One joint project published in late 2014 was on reducing the pessimism in BEOL timing signoff. WNS was reduced by 100ps and the methodology is in production use now. The work on using multiple libraries with different cell heights for the same block, which I covered a few weeks ago here, also produced impressive results such as 25% area reduction and 20% frequency increase.

- **WNS and TNS are reduced by up to 100ps and 53ns**
- **In production now ☺**



Successful projects have several factors in common:

- Target only real, critical problems
- Well-defined delivery spec
- Sufficient resources, especially advanced technology information and design databases
- Disciplined project management
- Good and open communication

The biggest issues facing traditional academic EDA research seem to be not knowing the critical problems that need the most attention, and not having access to true advanced libraries and process data. For the latter, there are "academic" libraries and designs that are available but they are often unrealistic, lacking MCMM, multiple-power domains, multiple-clock domains, memories, and more. This results in years of delay or simply that "good" academic solutions such as sizers, cannot be used in real designs since they are only "good" in the context of the academic benchmarks that are available. EDA startup companies often suffer from this symptom, too, since Samsung and Qualcomm are probably not giving you their leading-edge designs to use as test cases.

cadence ACADEMIC NETWORK

But EDA in general, and Cadence in particular, does do some things right. Tool availability means that students use the same tools and flows as industry. Making the Cadence online training available is a real game changer. Around 60 students in his graduate SoC implementation methodology class earlier this year had to take online STA and P&R trainings as part of the course, and it is, by definition, industrial strength.

Students also have access to the Cadence online community.

Another game changer is making large numbers (hundreds) of licenses available for research, including support for advanced technology nodes. With this, Kahng's lab has for many years used machine learning and optimization-centric methods to improve analysis correlation and implementation QOR.

So the overall conclusion is that things are improving but could still be better. There are existence proofs of successful collaboration. The speed at which semiconductor and EDA technology advances means that we can't afford unforced multi-year delays due to poor policies, poor data availability and openness, poor interoperability, and so on.

Summarizing the whole talk, I would say that the biggest issues are:

- Lack of real-world test data (PDKs, real designs, real libraries)
- Lack of communication that can keep students focused on "right problems" as opposed to "wrong problems"
- Duplication of effort since there is a lack of open source implementations of non-competitive stuff like LEF/DEF, SPEF or Verilog readers, or Liberty characterizers
- Academia needs money and company engagement to attract good students, but research is unpredictable by definition, so having a solid return-on-investment analysis ahead of the project is hard
- Confidentiality/NDA/conflict-of-interest policies can get in the way

Andrew's presentation is available on the **CDNLive Silicon Valley 2016 Proceedings** page.

Next: **3D Xpoint: Is It a Game-Changer?**

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