ECE260B – CSE241A
Winter 2004

Power Introduction

Website: http://vlsicad.ucsd.edu/courses/ece260b-w04
Power Dissipation

Lead Microprocessor's power continues to increase

Power delivery and dissipation will be prohibitive(?)

Courtesy, Intel
Power Density

- Rocket
- Nozzle
- Nuclear Reactor
- Hot Plate
- Pentium® proc

Power density too high to keep junctions at low temp(?)

Courtesy, Intel
Power and Energy Figures of Merit

- **Power** consumption in Watts
  - Determines battery life in hours
  - Energy density ~120W-hrs/kg

- **Peak power**
  - Determines power ground wiring designs
  - Sets packaging limits (50W/cm² ? 120W total ?) ($1/Watt ?)
  - Impacts signal noise margin and reliability analysis (Why?)

- **Energy efficiency** in Joules
  - Rate at which power is consumed over time

- **Energy = power * delay**
  - Joules = Watts * seconds
  - Lower energy number means less power to perform a computation at the same frequency
Power Versus Energy

Power is height of curve

Lower power design could simply be slower

Energy is area under curve

Two approaches require the same energy
Power dissipation in static CMOS gate: 3 components

- **Dynamic capacitive (switching, “useful”) power**
  - Still dominant component in current technology
  - Charging and discharging the capacitor

- **Crowbar current (short-circuit power)**
  - During a transition, current flows through both P and N transistors simultaneously for a SHORT period of time
  - Slow transitions worsen short-circuit power

- **Leakage (“useless power”) current**
  - Even when a device is nominally OFF ($V_{GS}=0$), a small amount of current is still flowing
  - With many devices, can add up to hundreds of mW
Reducing Dynamic Capacitive (Switching) Power

\[ P_{\text{dyn}} = C_L V_{DD}^2 P_0 \rightarrow f \]

Capacitance: Function of fan-out, wire length, transistor sizes

Activity factor: How often, on average, do wires switch?

Supply Voltage: Has been dropping with successive generations

Clock frequency: Increasing...

Slide courtesy of Mary Jane Irwin, PSU
Crowbar (Short-Circuit) Current

- Finite slope of the input signal causes a direct current path between $V_{DD}$ and GND for a short period of time during switching when both the NMOS and PMOS transistors are conducting.

- When $V_{TN} < V_{IN} < V_{DD} + V_{TP}$
  - Both transistors are ON
  - Current flowing directly from $V_{DD}$ to $V_{GND}$ is crowbar current

- Usually not a problem, e.g.,
  - P is ON strongly (LIN but with small $V_{DS}$ if at all)
  - N is barely ON
Leakage (Inactive, “Useless”) Power

- Three sources of leakage

- The dominant is the Source-to-Drain leakage current
  - Even when $V_{GS} = 0$, a small amount of charge is still present under the gate
  - Exponentially related to the gate (and S/D) voltage

\[ I_D \propto \frac{W}{L} \exp\left(\frac{q(V_{GS} - V_T)}{nkT}\right) \]

- Source/Drain are junctions and some amount of reverse bias, $I_S$ is present
  - Typically much smaller than S/D leakage

- Gate tunneling leakage
  - When $t_{ox}$ is only 5-10 atoms, easy for tunneling current to flow
  - More of an issue sub 0.10-μm technology
2001 ITRS Projections of 1/τ and I_{sd,leak} for HP, LP Logic

- **1/τ** (GHz)
- **I_{sd,leak}** (µA/µm)


- **1/τ** — High Perf.
- **I_{sd,leak}** — High Perf.
- **1/τ** — Low Pwr
- **I_{sd,leak}** — Low pwr

- **1** × 10^{-06}
- **1** × 10^{-05}
- **1** × 10^{-04}
- **1** × 10^{-03}
- **1** × 10^{-02}
- **1** × 10^{-01}
- **1** × 10^{00}
- **1** × 10^{01}
- **1** × 10^{02}
- **1** × 10^{03}
- **1** × 10^{04}
- **1** × 10^{05}
- **1** × 10^{06}
Projections for Low Power Gate Leakage

• Need for high K driven by Low Power, not High Performance
Summary: Power and Energy Equations

\[ E = C_L V_{DD}^2 P_{0\rightarrow1} + t_{sc} V_{DD} I_{\text{peak}} P_{0\rightarrow1} + V_{DD} I_{\text{leakage}} \]

\[ P = C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{\text{peak}} f_{0\rightarrow1} + V_{DD} I_{\text{leakage}} \]

Dynamic power
\((\sim90\% \text{ today and decreasing relatively})\)

Short-circuit power
\((\sim8\% \text{ today and decreasing absolutely})\)

Leakage power
\((\sim2\% \text{ today and increasing relatively})\)

Designers need to comprehend issues of memory and logic power, speed/power tradeoffs at the process (HiPerf vs. LowPower) level,