Sequential circuits
- Combinational circuits + storage elements

A sequential circuit takes input and generates output based on the current state of the system.

Sequential circuits are of two types
- Synchronous sequential circuits
  - Use clock input. Output changes with reference to clock.
- Asynchronous sequential circuits
  - Do not use clock input.

LATCHES

Latches are sequential circuits that remain in a state indefinitely until directed by an input signal.

S-R Latch (using NOR gates)

\[
\begin{array}{c}
\text{S} \\
\hline
0 & 0 & \text{Q} \\
0 & 1 & 0 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

- S = RESET
- R = SET

Output will be RESET
Output will be SET
Undefined state
\[ \overline{S\bar{R}} \text{latch (using NAND gates)} \]

Note that positions of \( S, R \) are swapped from that of SR latch.

\[
\begin{array}{c|c|c|c|c}
 S & R & Q & \bar{Q} \\
\hline
 0 & 0 & ? & ? & \text{undefined} \\
 0 & 1 & 1 & 0 & \text{SET state} \\
 1 & 0 & 0 & 1 & \text{RESET state} \\
 1 & 1 & ? & ? & \text{No change from previous state} \\
\end{array}
\]

\[ S\bar{R} \text{latch with clock (or control) input} \]

This part of the circuit is the same as S\bar{R} latch above.

\[
\begin{array}{c|c|c|c|c|c|c}
 C & S & R & Q & \bar{Q} \\
\hline
 0 & X & X & ? & ? & \text{No change in state} \\
 1 & 0 & 0 & ? & ? & \text{No change in state} \\
 1 & 0 & 1 & 0 & 1 & \text{RESET} \\
 1 & 1 & 0 & 1 & 0 & \text{SET} \\
 1 & 1 & 1 & ? & ? & \text{Undefined} \\
\end{array}
\]

Observe the differences between \( S\bar{R} \) latch, S\bar{R} latch, and \( S\bar{R} \) latch (with control input).

Undefined state is a state in which the \( Q \) and \( \bar{Q} \) outputs are 0 or 1 simultaneously.

Note that for \( S\bar{R} \) latch and \( S\bar{R} \) latch (with control input), \((S=0, R=0)\) does not produce any change in the outputs \( Q \) and \( \bar{Q} \). Whatever their values were previously will remain.
D latch

D latch is an SR latch with \( R = \overline{S} \)

The undefined state in SR latch can be eliminated in D latch.

Observe that when \( D = 1 \), the input to NAND gate 1 is 1 and input to NAND gate 2 is 0

when \( D = 0 \), input to NAND gate 1 is 0 and input to NAND gate 2 is 1.

We avoid the occurrence of input combination 1 1

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
<th>Next state of Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>No change from previous state</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>( \beta = 0 ) ( \rightarrow ) RESET</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>( \beta = 1 ) ( \rightarrow ) SET</td>
</tr>
</tbody>
</table>

Q: What is the difference between a latch and a flip-flop?