RAM Integrated Circuits

- \( m \) words \( \times \) \( n \) bits per word \( \Rightarrow \) \( mn \) binary storage cells
- \( \log_2 m \) address lines select a word (bitcells)

Example: 1K \( \times \) 16 memory

\[ 2^{10} \times 2^4 = 2^{14} \text{ bits} = 2 \text{ KBytes} \]

- Bitcell

SRAM: SR latch with select enable

(See: Bitslice, Figure 6-6)

- 16 \( \times \) 1 RAM

3-state ("tri-state") output buffer

<table>
<thead>
<tr>
<th>EN</th>
<th>IN</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>01</td>
<td>11</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
<td>01</td>
</tr>
</tbody>
</table>
• Large memories: decoder size is too large
  \[ \Rightarrow 2^k \text{ AND gates with } k \text{ inputs per AND} \]

Solution: • 2-dimensional array of RAM cells
  
  • Separate decoders for row, column
  
  • See Figures 6-10, 6-11

Example: Given a \[ 4 \times 4 \] RAM array of RAM cells

Not a \[ 4 \times 4 \text{ RAM} \]
• Large memories: decoder size is too large

\[ 2^k \text{ AND gates with } k \text{ inputs per AND} \]

Solution: 2-dimensional array of RAM cells
- Separate decoders for row, column
- See Figures 6-10, 6-11

Example: Given a 4x4 RAM cell array

Not a “4x4 RAM”

16x1 RAM

A1, A0

Chip Select
Large memories: decoder size is too large

$2^k$ AND gates with $k$ inputs per AND

Solution: 2-dimensional array of RAM cells
- Separate decoders for row, column
- See Figures 6-10, 6-11

Example: Given a 4x4 RAM array of RAM cells

Not a "4x4 RAM"
Given: 256 x 4 RAM's

- Build 512 x 4 RAM

- Build 256 x 8 RAM
Given: 256 x 4 RAM's

- Build 512 x 4 RAM

- Build 256 x 8 RAM