50 MHz clock → 20ns clock period

Write cycle 75ns

- Give address, enable memory at T1
- Data provided at T2
- R/W signal changes at T2 after signals on address lines have become fixed
- R/W signal must stay at 0 until 75ns after address, memory enable applied
- Address, data signals remain stable until after R/W goes to 1.

If not: ?
Read cycle 65 ns

- CPU applies address, sets Memory Enable to 1, sets R/W to 1 (at T1)
- Data is placed onto data output lines within 65 ns
- CPU can then transfer data to an internal register at next clock pulse (T1)
RAM Bitslice

- Bitslice = set of RAM cells + circuitry associated w/ bit position
- Loading controlled by Word Select input
- If Bit Select = 1 and Word Select = 1

Fig 6-6 RAM Bit slice model
RAM Bit slice symbol