PD: Verification Vs. Modification

- IO Pad Placement: estimated
- Power/Ground Stripes, Rings Routing: easy
- Placement: accurate
- Clock Tree Synthesis: difficult
- Global Routing
- Detail Routing
- ‘Post’-layout Optimization
- Extraction and Verification

Not real post-layout optimization, but a new PD loop…
TEG: A Post-layout Optimization Method

Detail Routing → Geometry Layout

Geometry Layout

Topological Layout

Extraction & Verification

Topological DRC

DRV Solver

DRVS

Layout Modification

Post-layout Optimization

To be appeared in ISPD'02
Wire Sizing by TEG

Original Layout (LEF/DEF)

After wire sizing (LEF/DEF)

Fix crosstalk-delay, reduce IR-drop …
Wire Distribution by TEG

Original Layout

After wire distribution

Decrease CMP process variation, improve yield and manufacturability…