Benchmark Update

◆ Carnegie Cell Library: “Free to all who Enter”
  - Need to build scaling model of standard cell library
  - Based on our open 0.35 micron library (real extracted data)
  - This semester: basic standard cells
  - This summer: memories

◆ Timing Models
  - Actual timing probably is not as important as variations
  - Simple 1-order models of speed and variations
New vertical benchmarks:

- All designed to comply with common network interface
- Interoperability, portability for IP blocks
- Why is this interesting/useful for benchmarks?
  - IOs and other system-level issues make it hard to compare benchmarks
- Also good for education
New Circuit Benchmarks

◆ The Network Tile: for streaming applications

◆ The Processing Elements:
  - Morphable Floating Point Multiplier:
    ♦ FP mult and vector add, integer multiply and integer MAC and shift
  - Morphable Floating Point Adder:
    ♦ FP add and integer add and shift
  - Programmable Integer ALU
  - Programmable FIR filter
  - SIMD Adder (with funky completion logic)

◆ All about 20-100k gates each
  - Can be combined into systems of arbitrary size
  - Network limits effective Rent’s Exponent
  - *Actually Network connectivity would determine Rent Exponent
    ♦ Currently planning 2-D network, creating Rent Exponent of 0.5
Dynamic Network Tiles

TILE: the network component

PE: the component at this node in the network
Dynamic Network System

Reference Clock distribution through network
Each tile generates own clock
Interface decoupled via FIFOs

New Placement Problem:
space utilization vs. distance
Target Architecture:

Pipelined Arrays

- Limited Feedback
- Long/short wires predictable
- Clock Skew
- Important Application Domain
Classic Wire Length Models
Wire Path Length

- Every block is a pipeline stage
- Impossible to determine every wire length from floorplan blocks
- Wire Path Length (WPL) measures the distance between consecutive registers
Results Key

- **Classic**
  - Different random starting position every time
  - Classic Move Set - Swap

- **Classic + LSP**
  - Same legal starting position every time
  - Classic Move Set - Swap

- **New**
  - Same legal starting position every time
  - New Move Set - Insert/Delete
1-D DCT

- 12 Pipeline Stages

- Synthesis Speed - 2.25 ns.

- Synthesis Area - 668,323 $\mu$m$^2$
Unfloorplanned
Classic + LSP
## Results

<table>
<thead>
<tr>
<th></th>
<th>Dead Space</th>
<th>WPL</th>
<th>DRCs</th>
<th>Speed</th>
<th>Avg. Cong.</th>
<th>Max Cong.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>No Floor</strong></td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>2.50</td>
<td>0.35</td>
<td>0.98</td>
</tr>
<tr>
<td><strong>Classic</strong></td>
<td>0.97%</td>
<td>6.15</td>
<td>850</td>
<td>2.40</td>
<td>0.60</td>
<td>1.32</td>
</tr>
<tr>
<td><strong>Classic + LSP</strong></td>
<td>1.63%</td>
<td>5.88</td>
<td>138</td>
<td>2.44</td>
<td>0.57</td>
<td>1.31</td>
</tr>
<tr>
<td><strong>New</strong></td>
<td>0.09%</td>
<td>5.76</td>
<td>12</td>
<td>2.37</td>
<td>0.54</td>
<td>1.19</td>
</tr>
</tbody>
</table>