**강 석 형 조교수**
**Seokhyeong Kang**

School of Electrical and Computer Engineering,
Ulsan National Institute of Science and Technology (UNIST)

### Curriculum Vitae

- 2014~Present: Assistant Professor, UNIST
- 2013~2014: Staff Engineer, ASIC Design Automation, Qualcomm Technologies, Inc.
- 2001~2008: Senior Engineer, SoC Development Team, Samsung Co., LTD.

### Academic Credential

- 2013: Ph. D. Electrical and Computer Engineering, University of California, San Diego
- 2001: M. S Electrical Engineering, POSTECH
- 1999: B. S. Electrical Engineering, POSTECH

### Awards/Honors/Memberships

- First place at the ISPD Discrete Gate Sizing Contest, 2013

### Research Groups

# Low Power System-on-Chip Design Lab.

In System-on-Chip (SoC) design, increasing thermal densities and the portability of emerging computing systems demand further reduction of design power. However, in integrated-circuit (IC) designs, there is a tradeoff between energy and performance, and the solution space for any given design is bounded by the lowest possible energy and the highest possible performance. To extend the achievable energy-performance envelope, Low Power SoC Design Lab is focused on system- and design-level techniques such as (i) error-resilient design, (ii) dynamic voltage and frequency scaling (DVFS), (iii) approximate arithmetic design, and (iv) adaptive power gating. Our research proposes innovative techniques which exploit the system and application information, and connect them into design optimization and physical implementation to enable more energy-efficient designs.


### Research Keywords

System-on-Chip, Low Power, Computer-aided Design, Physical implementation

### Research interests

Energy-efficient SoC/VLSI design, adaptive and resilient design,
system and application-aware optimization, IC physical implementation

### On going research Topics (selected)

1. Exploiting error resilience in low-power design
2. Approximate arithmetic design

### Research Publications (selected)

1. Andrew B. Kahng, Seokhyeong Kang, Tajana S. Rosing and Richard Strong, “Many-Core Token-Based Adaptive Power Gating”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 32(8) (2013), pp. 1288–1292.
2. Andrew B. Kahng, Seokhyeong Kang, Rakesh Kumar and John Sartori, “Enhancing the Efficiency of Energy-Constrained DVFS Designs”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 21(10) (2013), pp. 1769–1782.
3. Andrew B. Kahng, Seokhyeong Kang, Hyein Lee, Igor L. Markov and Pankit Thapar, “High-Performance Gate Sizing with a Signoff Timer”, Proc. IEEE/ACM International Conference on Computer-Aided Design, 2013, pp. 450–457.
4. Andrew B. Kahng, Seokhyeong Kang, Rakesh Kumar and John Sartori, “Recovery-Driven Design: Exploiting Error Resilience in Design of Energy-Efficient Processors”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 31(3) (2012), pp. 404–417.
5. Andrew B. Kahng and Seokhyeong Kang, “Accuracy-Configurable Adder for Approximate Arithmetic Designs”, Proc. ACM/IEEE Design Automation Conference, 2012, pp. 820–825.

### Patents (selected)

1. Seokhyeong Kang, “Device and Method for Determining a Defective Area on an Optical Media” U.S. 7849379, Taiwan 2006-38413, Japan 2006-164503, France 2879011-A1.
2. Seokhyeong Kang, “Defect Judgment Apparatus for the Optimized defect Process of an Optical Storing Medium”, Korea 102004-0102362.