PUNEET SHARMA

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Research Interests

- Physical design techniques for manufacturability and yield enhancement
- Power analysis and optimization

Education

- Ph.D. in Electrical and Computer Engineering, University of California, San Diego
  Expected graduation: July 2007
  Thesis: Manufacturing-Aware Physical Design Techniques
  Advisor: Prof. Andrew B. Kahng
- B.Tech. (2002) in Computer Science and Engineering, Indian Institute of Technology, Delhi
  Thesis: Lightfield Rendering

Professional Experience

- **Freescale Semiconductor** Austin, TX *(Jun '06 – Sep '06)*
  - Worked with the PowerPC design team involved in power analysis and optimization.
  - Designed and implemented a high-level power analysis tool.
  - Designed a temperature-aware power analysis and optimization methodology.
- **Blaze DFM, Inc.** Sunnyvale, CA *(Feb '05 – Sep '05)*
  - Worked on design and implementation of tools for: (1) leakage optimization, (2) systematic variation-aware analysis and optimization, (3) lithography simulation-based design analysis, and (4) variation-aware library characterization.
- **University of California** San Diego, CA *(Sep '02 – present)*
  - My past and ongoing research is in several areas: (1) systematic variation-aware design analysis and optimization, (2) leakage power optimization, (3) metal-layer and STI dummy fill insertion and its performance impact, and (4) timing and power analysis, and parasitic extraction.
- **University of Dortmund** Dortmund, Germany *(May '01 – Jul '01)*
  - Advisors: Prof. Peter Marwedel and Prof. Rainer Leupers
  - Worked with the retargetable compiler group on runtime optimization.

Career Highlights

- **Research at UCSD**
  - Published several papers in the area of VLSI design automation (two journal papers, six papers in top-tier conferences, and seven papers in other conferences).
  - Leakage and leakage variation reduction technique developed by me and my UCSD collaborators commercialized by Blaze DFM, Inc. (http://www.blaze-dfm.com).
  - Blurb in MIT's Technology Review magazine of Oct, 2004 on PhoneShare, a P2P internet telephony technology developed by me and my advisor. IP and software rights transferred by UCSD to Intellectual Ventures.
- **Internships**
  - Freescale Semiconductor. Two invention disclosures filed in the area of power analysis and are under Freescale's internal review process.
  - Blaze DFM, Inc. Designed and developed key software components; filed two patent applications; was part of a three-member team that reduced leakage power of a taped-out Qualcomm design by over 20% (details at http://www.chipdesignmag.com/display.php?articleId=475).

Publications and Talks

Note: Papers coauthored with my advisor Prof. Andrew Kahng have authors listed in alphabetical order.

Journal Articles

- A. B. Kahng, S. Muddu and P. Sharma, "Defocus-Aware Leakage Estimation and Control," in *IEEE Trans. on Computer-Aided Design*, **TCAD** 2007, to appear.
- P. Gupta, A. B. Kahng, P. Sharma and D. Sylvester, "Gate-Length Biasing for Runtime Leakage Control," in *IEEE Trans. on Computer-Aided Design*, Vol. 25, No. 8, **TCAD** 2006, pp. 1475 - 1485.
- P. Gupta, A. B. Kahng, I. Mandoiu and P. Sharma, "Layout-Aware Scan Chain Synthesis for Improved Path Delay Fault Coverage," in *IEEE Trans. on Computer-Aided Design*, Vol. 24, No. 7, **TCAD** 2004, pp. 1104 - 1114.

Conference Papers

- A. B. Kahng, P. Sharma and R. O. Topaloglu, "Exploiting STI Stress for Performance," in *Proc. Intl. Conf. on Computer-Aided Design*, **ICCAD** 2007, to appear.
- A. B. Kahng, S. Muddu and P. Sharma, "Detailed Placement for Leakage Reduction using Systematic Through-Pitch Variation," in *Proc. Intl. Symp. on Low Power Electronics and Design*, **ISLPED** 2007, to appear.
- A. B. Kahng, S. Reda and P. Sharma, "On-Line Adjustable Buffering for Runtime Power Reduction," in *Proc. Intl. Symp. on Quality Electronic Design*, **ISQED** 2007, pp. 550 - 555.
- A. B. Kahng, P. Sharma and A. Zelikovsky, "Fill for Shallow Trench Isolation CMP," in *Proc. Intl. Conf. on Computer-Aided Design*, **ICCAD** 2006, pp. 661 - 668.
- A. B. Kahng, S. Muddu and P. Sharma, "Impact of Gate-Length Biasing on Threshold-Voltage Selection," in *Proc. Intl. Symp. on Quality Electronic Design*, **ISQED** 2006, pp. 747 - 754.
- A. B. Kahng, K. Samadi and P. Sharma, "Study of Floating Fill Impact on Interconnect Capacitance," in *Proc. Intl. Symp. on Quality Electronic Design*, **ISQED** 2006, pp. 691 - 696.
- A. B. Kahng, C.-H. Park, P. Sharma and Q. Wang, "Lens Aberration-Aware Placement for Across Field Line-Width Control," in *Proc. Design Automation and Testing in Europe*, **DATE** 2006, pp. 890 - 895.
- P. Gupta, A. B. Kahng and P. Sharma, "Lithography Simulation-Based Full-Chip Design Analyses," in *Proc. SPIE Conference on Microlithography*, **Microlithography** 2006, pp. 61560T-1 – 61560T-8.
- A. B. Kahng, S. Muddu and P. Sharma, "Defocus-Aware Leakage Estimation and Control," in *Proc. Intl. Symp. on Low Power Electronics and Design*, **ISLPED** 2005, pp. 263 - 268.
- P. Gupta, A. B. Kahng and P. Sharma, "A Practical Transistor-Level Dual Threshold Voltage Assignment Methodology," in *Proc. Intl. Symp. on Quality Electronic Design*, **ISQED** 2005, pp. 421 - 426.
- P. Gupta, A. B. Kahng, C.-H. Park, P. Sharma, D. Sylvester and J. Yang, "Joining the Design and Mask Flows for Better and Cheaper Masks," invited paper in *Proc. 24th BACUS Symposium on Photomask Technology and Management*, **BACUS** 2004, pp. 318 - 329.
- P. Gupta, A. B. Kahng, P. Sharma and D. Sylvester, "Selective Gate-Length Biasing for Cost-Effective Runtime Leakage Control," in *Proc. Design Automation Conference*, **DAC** 2004, pp. 327 - 330.
- P. Gupta, A. B. Kahng, I. Mandoiu and P. Sharma, "Layout-Aware Scan Chain Synthesis for Improved Path Delay Fault Coverage," in *Proc. Intl. Conf. on Computer-Aided Design*, **ICCAD** 2003, pp. 754 - 759.

Non-VLSI Publications

- P. Sharma, A. Parashar, S. Banerjee and P. Kalra, "An Uncalibrated Lightfield Acquisition System," in *Journal of Image and Vision Computing*, Elsevier Publications, Vol. 22, pp. 1197 - 1202, 2004.
- P. Sharma, A. Parashar, S. Banerjee and P. Kalra, "An Uncalibrated Lightfield Acquisition System," in *Indian Conf. on Computer Vision, Graphics and Image Processing*, 2002.

Patents and Invention Disclosures

- P. Gupta, A. B. Kahng, S. Muddu and P. Sharma, "Method and System for Topography-Aware Integrated Circuit Design Analysis and Optimization" (with Blaze DFM, Inc.).
- P. Gupta, A. B. Kahng, S. Shah and P. Sharma, "System and Method for Standard-Cell Library Optimization" (with Blaze DFM, Inc.).
- J. Cox, A. B. Kahng and P. Sharma, "Internet Telephony Through Hosts," Patent Application No. 20070005729 (with UCSD).

Conference Talks

- "On-Line Adjustable Buffering for Runtime Power Reduction, " ISQED07.
- "Fill for Shallow Trench Isolation CMP," ICCAD06.
- "Study of Floating Fill Impact on Interconnect Capacitance," ISQED06.
- "Selective Gate-Length Biasing for Cost-Effective Runtime Leakage Control," DAC04.
- "Layout-Aware Scan Chain Synthesis for Improved Path Delay Fault Coverage," ICCAD03.

Awards and Honors

- UCSD departmental fellowship for 2002-2003.
- Senior thesis nominated for the best undergraduate project award.
- All India Rank **36** out of over 150,000 examinees in the Joint Entrance Examination for the Indian Institutes of Technology (IIT-JEE 1998).
- Ranked 29 in National Science Talent Search, India, 1994.
- Ranked 20 in National Science Talent Search, India, 1993.

Service

- Reviewer for: Intl. Conf. on Computer-Aided Design; Design Automation Conference; Intl. Symp. on Physical Design; Intl. Workshop on Design for Manufacturability and Yield; IEEE Trans. on VLSI; IEEE Trans. on Computers.
- Teaching assistant for graduate-level course titled "VLSI Integrated Circuits and Systems Design".
- Helped my advisor Prof. Kahng with funding proposals to SRC and NSF.
- System administration of our research group's computing cluster with 25 servers and workstations running Linux with shared filesystems, central authentication, email, tape backups, etc.

Graduate-Level Courses

- Algorithm design and analysis; combinatorial algorithms; computer architecture; operating systems; advanced compiler design; algorithmic foundations of VLSI CAD; VLSI integrated circuits and systems design; VLSI physical design and design-manufacturing interface; nanometer-scale VLSI devices; embedded software; advanced networks.

Computing Skills

- **Programming languages:** C/C++ (expert), Perl (intermediate), Java (intermediate).
- **Platforms:** Expertise in Linux usage and system administration, Solaris.
- **EDA tools:** Familiarity with Mentor Calibre, ModelSim, Cadence NC-VHDL, Cadence BuildGates, Cadence Soc Encounter, Synopsys DesignCompiler, Synopsys PrimeTime, Synopsys TetraMAX.
- **Other languages/tools:** OpenAccess, Verilog, Lex, Yacc, HTML, AJAX, Matlab.
- **Software developed:** Static timing analyzer, detailed placer, leakage optimizer (licensed by UCSD), scan-chain optimizer, P2P VoIP with PSTN interface (licensed by UCSD), etc.

Work authorization: Presently on F1 visa, H1-B visa approved for 2008. Updated: 29 June, 2007.
References available upon request.