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Education

• Ph.D.	Computer Science	U.C. San Diego	expected 2006
• M.S.	Computer Software and Theory	Tsinghua Univ., P.R. China	2001
• B.Eng.	Computer Science and Technology	Tsinghua Univ., P.R. China	1998

Ph.D. Dissertation: " Analytical Methods for VLSI Module Placement", Prof. Andrew B. Kahng

We propose and implement APlace, a general analytical placement framework, which has high solution quality and strong extensibility. APlace regards global placement as a constrained nonlinear optimization problem, applies smooth approximations of placement objectives and density functions, and solves the problem using the Quadratic Penalty method and a Conjugate Gradient solver. The general APlace framework has been extended to address a variety of placement tasks, such as mixed-size placement, timing-driven placement, power-aware placement, voltage-drop-aware placement, aberration-aware timing-driven placement and I/O-core co-placement, and is shown to be competitive in a wide variety of contexts.

Honors and Awards

- **Best Paper nomination,** Intl. Conf. on Computer-Aided Design 11/2005
- **Best Paper award**, Intl. Conf. on Computer Design 10/2005
- **First Place**, Intl. Symp. Physical Design 2005 Placement Contest 04/2005
- **Jacob Fellowship**, U.C. San Diego 2001-2002

Research Experience

- A general analytical placement framework and its extensions to mixed-size placement, timing-driven placement and congestion-directed placement.
- A placement method with awareness of lens aberration effects for timing yield optimization.
- A placement method of relocating cells for supply voltage drop improvement.
- A placement method with clock register clustering and activity-based net weighting for clock power and switching power reduction.
- A novel detail placement algorithm.
- Planning of hierarchical, uniform power distribution in early design stages, with optimization for worst IR-drop or total metal area.
- Analysis of key deployment and methodology issues associated with the Y-architecture for on-chip interconnect (three uniform routing directions), including throughput analysis, estimates of wirelength savings, clock and power distribution, wireability, and manufacturing.

Relevant Work Experience

• Research Assistant	U.C. San Diego	09/2002-present
• Student Intern	Advanced Technology Group, Synopsys Inc.	06/2004-09/2004
• Research Assistant	Tsinghua Univ.	09/1998-06/2001

Teaching Experience

• Teaching Assistant	Mathematics for Algorithm and Systems	UCSD	Winter, 2006
• Teaching Assistant	Software Engineering (Graduate)	Tsinghua	03/2000-07/2000
• Teaching Assistant	Software Engineering	Tsinghua	09/1999-01/2000

Publications: *Authors are listed in alphabetical order; Presenters are marked for conference papers.*

Journal Articles

J5. A. B. Kahng, C.-H. Park, P. Sharma and Q. Wang, "Lens Aberration Aware Placement for Timing-Improvement", submitted to **IEEE Transactions on Computer-Aided Design.**

J4. A. B. Kahng, S. Reda and Q. Wang, "Anatomy of an Analytic Placer", submitted to **ACM Journal of Experimental Algorithmics**.

J3. A. B. Kahng, I. Mandoiu, Q. Wang, X. Xu, and A. Zelikovsky, "Multi-Project Reticle Floorplanning and Wafer Dicing"**,** accepted and to appear at **IEEE Transactions on Computer-Aided Design.**

J2. A. B. Kahng and Q. Wang, "Implementation and Extensibility of an Analytic Placer", **IEEE Transactions on Computer-Aided Design** 24(5) (2005), pp. 734-747.

J1. H. Chen, C. K. Cheng, A. B. Kahng, I. Mandoiu, Q. Wang, and B. Yao, "The Y-architecture for On-Chip Interconnect: Analysis and Methodology", **IEEE Transactions on Computer-Aided Design** 24(4) (2005), pp. 588-599.

Selected Conference Papers

C10. A. B. Kahng, C.-H. Park, P. Sharma and Q. Wang, "Lens Aberration Aware Timing-Driven Placement", **Proc. Design, Automation and Test in Europe**, March 2006, to appear.

C9. **A. B. Kahng***, S. Reda and Q. Wang, "Architecture and Details of a High Quality, Large-Scale Analytical Placer", **Proc. Intl. Conf. on Computer-Aided Design**, 2005, pp. 891-898. (**Best Paper nominee**)

C8. A. B. Kahng, B. Liu and **Q. Wang***, "Supply Voltage Degradation Aware Placement", **Proc. Intl. Conf. on Computer Design**, 2005, pp. 437-443. (**Best Paper award**)

C7. Y.-S. Cheon, P.-H. Ho, A. B. Kahng, S. Reda, and **Q. Wang***, "Power-Aware Placement", **Proc. Design Automation Conference**, 2005, pp. 795-800.

C6. **A. B. Kahng***, S. Reda and Q. Wang, "APlace: A General Analytic Placement Framework", **Proc. Intl. Symp. Physical Design**, 2005, pp. 233-235. (Short Paper)

C5. A. B. Kahng and **Q. Wang***, "An Analytic Placer for Mixed-Size Placement and Timing-Driven Placement", **Proc. Intl. Conf. Computer-Aided Design**, 2004, pp. 565-572.

C4. A. B. Kahng and **Q. Wang***, "Implementation and Extensibility of an Analytic Placer", **Proc. Intl. Symp. Physical Design**, 2004, pp. 18-25.

C3. A. B. Kahng, I. Mandoiu, Q. Wang, X. Xu*, and A. Zelikovsky, "Multi-Project Reticle Floorplanning and Wafer Dicing", **Proc. Intl. Symp. Physical Design**, 2004, pp. 70-77.

C2. H. Chen, **C. K. Cheng***, A. B. Kahng, M. Mori, and Q. Wang, "Optimal Planning for Mesh-Based Power Distribution", **Proc. Asia and South Pacific Design Automation Conference**, 2004, pp. 444-449.

C1. H. Chen, C. K. Cheng, A. B. Kahng, I. Mandoiu, **Q. Wang***, and B. Yao, "The Y-architecture for On-Chip Interconnect: Analysis and Methodology", **Proc. Intl. Conf. Computer-Aided Design**, 2003, pp. 13-19.

References

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