When 10M Gates Just Isn’t Enough ... The GPU Challenge

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GeForce 4 Ti

World’s Most Powerful GPU

- Lightspeed Memory Architecture II
  - 2nd Generation Occlusion Culling
  - Lossless 4:1 Compression
  - Quadcache Architecture

- Worlds fastest DDR memory
  - 650 MHz data rates
  - 10.4 GB/sec memory bandwidth

- 128MB Frame Buffer
  - Enables next-generation content
  - High resolution AA requires large frame buffers
  - 1600 x 1200 4x FSAA doesn’t fit in 64MB

- Advanced processor design
  - 300 MHz core & 325 Mhz memory clock
  - 63M transistors
  - 100 days from tapeout to production
- 0.15u, 8LM, 63M txtr, 505 signals/801 balls, 18W
Where Did all the Transistors Go?

- Logic: 78% of die
- Memory: 20% of die
- DACs/PLLs: 2% of die

Example
- GeForce4 memory controller
  - 4th generation of our DDR memory controller architecture
  - Area allocated to it has tripled (now about 9-10% of die)
- GeForce4 Pixel processing functions
  - over 50% of die
  - was only 20% 2 years ago (GeForce256)
GeForce4 Experience

- 63 Million transistors
- 6M txtr added over GeForce3, 40-50% of RTL changed or modified
- 9 month from POR to tapeout
- 101 days from tapeout to volume ramp
- 25% core clock speed improvement
- 18% memory clock improvement

- 19 functional problems initially reported
  - 7 required fixing, all in metal
- 1 problem related to a mixed signal component modeling error
- 2 performance related issues investigated and addressed
## Our Track Record

<table>
<thead>
<tr>
<th>Project</th>
<th>Time Frame</th>
<th>Approx Program Duration</th>
<th>Process Technology</th>
<th>Approx Transistors</th>
<th>Relative Staffing</th>
<th>Relative Algorithmic (ie Design) Complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td>NV1</td>
<td>1993-1994</td>
<td>1 1/2 yr</td>
<td>0.5u</td>
<td>3/4M</td>
<td>1x</td>
<td>1x</td>
</tr>
<tr>
<td>NV2</td>
<td>1995</td>
<td>3/4 yr</td>
<td>0.5u</td>
<td>1.25M</td>
<td>1.2x</td>
<td>1.5x</td>
</tr>
<tr>
<td>RIVA 128</td>
<td>1996</td>
<td>1 yr</td>
<td>0.35u</td>
<td>4M</td>
<td>1.6x</td>
<td>4x</td>
</tr>
<tr>
<td>RIVA TNT</td>
<td>1997</td>
<td>1 yr</td>
<td>0.31u</td>
<td>7.5M</td>
<td>1.7x</td>
<td>7x</td>
</tr>
<tr>
<td>RIVA TNT2</td>
<td>1998</td>
<td>3/4 yr</td>
<td>0.25u</td>
<td>9M</td>
<td>1.5x</td>
<td>10x</td>
</tr>
<tr>
<td>GeForce 256</td>
<td>1998-1999</td>
<td>1 1/2 yr</td>
<td>0.22u</td>
<td>22M</td>
<td>2.5x</td>
<td>20x</td>
</tr>
<tr>
<td>GeForce2</td>
<td>1999-2000</td>
<td>3/4 yr</td>
<td>0.18u</td>
<td>25M</td>
<td>1.5x</td>
<td>4x</td>
</tr>
<tr>
<td>GeForce3</td>
<td>1999-2000</td>
<td>1 1/2 yr</td>
<td>0.15u</td>
<td>57M</td>
<td>3.5x</td>
<td>30x</td>
</tr>
<tr>
<td>XGPU</td>
<td>2000-2001</td>
<td>3/4 yr</td>
<td>0.15u</td>
<td>60M</td>
<td>1.5x</td>
<td>35x</td>
</tr>
<tr>
<td>GeForce4</td>
<td>2000-2001</td>
<td>3/4 yr</td>
<td>0.15u</td>
<td>63M</td>
<td>3.0x</td>
<td>40x</td>
</tr>
<tr>
<td>NextGen</td>
<td>2001-2002</td>
<td>1 1/2 yr</td>
<td>0.13u</td>
<td>~120M</td>
<td>5.0x</td>
<td>50x</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Project</th>
<th>FCS Mask Set</th>
<th>Tapeout to Volume</th>
</tr>
</thead>
<tbody>
<tr>
<td>RIVA TNT2</td>
<td>A02</td>
<td>98 days</td>
</tr>
<tr>
<td>GeForce 256</td>
<td>A03</td>
<td>104 days</td>
</tr>
<tr>
<td>GeForce2/GTS</td>
<td>A03</td>
<td>102 days</td>
</tr>
<tr>
<td>GeForce/MX</td>
<td>A01</td>
<td>110 days</td>
</tr>
<tr>
<td>GeForce3</td>
<td>A03</td>
<td>118 days</td>
</tr>
<tr>
<td>XGPU</td>
<td>A03</td>
<td>120 days</td>
</tr>
<tr>
<td>GeForce4</td>
<td>A02</td>
<td>101 days</td>
</tr>
</tbody>
</table>
The Scale of GPU Development

<table>
<thead>
<tr>
<th>GPU</th>
<th>Technology</th>
<th>Transistors</th>
<th>Frequency</th>
<th>Placeable Instances</th>
<th>Flops</th>
<th>Models C vs V</th>
<th>Directed Arch Tests</th>
<th>GDS2 File size</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen1</td>
<td>0.25u</td>
<td>9M</td>
<td>125MHz</td>
<td>1M</td>
<td>~60K</td>
<td>90K/300K</td>
<td>300</td>
<td>800KB</td>
<td>6 W</td>
</tr>
<tr>
<td>Gen2</td>
<td>0.18u</td>
<td>25M</td>
<td>250MHz</td>
<td>1.5M</td>
<td>~200K</td>
<td>100K/300K</td>
<td>6000</td>
<td>2GB</td>
<td>10 W</td>
</tr>
<tr>
<td>Gen3</td>
<td>0.15u</td>
<td>57M</td>
<td>350MHz</td>
<td>3M</td>
<td>~500K</td>
<td>400K/800K</td>
<td>25000</td>
<td>4.5GB</td>
<td>12 W</td>
</tr>
<tr>
<td>Gen4</td>
<td>0.13u</td>
<td>~120M</td>
<td>450MHz</td>
<td>5.5M</td>
<td>~750K</td>
<td>700K/1.3M</td>
<td>50000</td>
<td>8GB</td>
<td>15 W</td>
</tr>
</tbody>
</table>

1 - dual edge clocking
The Investment

- $160M of CAD tools installed and online
- $40M Emulation installation
- Engineering Compute resources
  - Desktops: 225 Suns, 5000 x86/linux/NT PCs
  - Server CPUs: 450 Sparc/Solaris, 2700 x86/Linux/NT
  - 3.2 Tera bytes RAM, 55 Tera bytes of storage
Compute Resource Allocation

**Linux Farm**
- Functional Verification
- Verilog Design Source
- C++ Model Source

**Sun Farm**
- Synthesis
- Place and Route
- Timing Analysis
- Completed Design

**Graph**
- X-axis: 0, 500, 1000, 1500, 2000, 2500, 3000
- Y-axis: 0, 500, 1000, 1500, 2000, 2500, 3000
Key Activities in Achieving Functional Correctness

- Validation
  - is what you want to build something that you’d want?
  - cmodel sims, emulation, application traces, modeling/analysis, formal tools

- Verification
  - attempt to prove you’ve designed what you decided you want
  - cmodel vs RTL simulations/emulation, formal, test plans, coverage

- Characterization
  - determine if what you built is what you tried to design
  - measurements, actual vs theory, delivered results, compatibility

- Certification
  - close the loop – is what you’ve built what you needed?
  - QA, compatibility, field testing, App Testing, Customer Acceptance
Our Challenges

- Project Scope
  - has just about out stretched a single persons ability to understand it all and be enough of an expert to lead it appropriately

- Complexity Management
  - understanding the global implications of local decisions
  - Occam’s Razor

- Verification / Validation completeness

- Increasingly Higher Speed interfaces
Our Strengths

- Experience
  - understand challenges, anticipate problems/resources/tool needs/areas of concern
- Cultural Appreciation of Flexibility
- A proven, battle tested methodology
  - constantly being tested, questioned, improved
- Caliber of our design team, competitive nature of our business
- Breadth of IP
- Focus on exploiting “best practices”
Our Concerns

- Deep submicron affects and surprises
- Staying on top of the verification explosion
- Increasing productivity of the design team
- Cost of mistakes is exploding
- Concurrent chip, package/substrate, board design
- Managing on-chip noise
State of our Art (circa DAC 2000 and 2002)

- Always worried that we’re lucky and not good …
  - which leads to the desire to automate, measure, standardize

- We have gotten good enough at the majority of things that the problems that we have left once we hit silicon are really tough!!

- We are becoming increasingly biased toward simple/predictable versus optimal

- Absolutely still true – if you don’t test or check it, it doesn’t work!

- Our biggest problem is “getting it right”