IC Packaging and IO

Interconnecting ICs With Their Environment

Lecture 14: IC Packaging and IO

1. IC Manufacturing
2. CMOS Technology
3. ASIC – Structures & Design Flow
4. FPGA – Technology & Devices
5. HDLs and Synthesis
6. Digital Design Methodology
7. Simulation digital
8. Simulation analog/mixed
9. IC Production Test
10. HW/SW Design and Verification
11. μP, μC, DSP
12. Comparing ASIC/FPGA vs. μP/μC
13. Managing ASIC-Projects
14. IC Packaging and IO
15. Future Trends
Contents

- Why IC packaging is that important
- Highlights the criteria for selecting packages and IO standards
- Introduces the basic well known IC packages
- Introduce the basic IO standards used today

IC Packages

- What is an IC package?

Source: Toshiba ASIC packaging
IC Packages

- What is an IC package?
  - More details
Why Packaging ICs?

- Pure silicon die is difficult to handle
  - Die is very fragile
  - Die is very small

- IC package is some sort of mechanical interface of the die and it’s environment
  - Prevent from damages during
    - Manufacturing (i.e. soldering)
    - Normal use

Why Packaging ICs?

- IC package prevents the die from electrical stress
  - EMC
  - UV light
    - EEPROM
  - X-rays
    - Space conditions, avionic environment
  - α- and γ-rays
    - Space conditions, avionic environment
Packaging Requirements

- **Speed**
  - Short chip-to-chip propagation delays
  - High bandwidth

- **Pin count and wireability**
  - Large IO count per chip edge
  - Dense wiring

- **Size**
  - Compact size to reduce board space

Packaging Requirements

- **Noise**
  - High quality transmission lines (large $Z_0$, low resistance)
  - Low noise coupling among wires
  - Power distribution with low inductance to minimize simultaneous switching noise
  - Power distribution with low resistance to achieve small IR drops
Packaging Requirements

- Thermal and mechanical
  - High heat removal rate
  - Good match between thermal expansion coefficients of the dice and the chip carrier
  - Prevent the die from destruction

- Test, reliability, cost
  - Easy to manufacture, test, modify and fix
  - Highly reliable
  - Low cost

Metals Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>thermal conductivity W/(cmK)</th>
<th>coefficient of thermal expansion 10^-6/K</th>
<th>electrical resistance μΩ/cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver</td>
<td>4,3</td>
<td>19</td>
<td>1,6</td>
</tr>
<tr>
<td>Copper</td>
<td>4,0</td>
<td>17</td>
<td>1,7</td>
</tr>
<tr>
<td>Aluminium</td>
<td>2,3</td>
<td>23</td>
<td>2,8</td>
</tr>
<tr>
<td>Tungsten</td>
<td>1,7</td>
<td>4,6</td>
<td>5,3</td>
</tr>
<tr>
<td>Molybdenum</td>
<td>1,4</td>
<td>5,0</td>
<td>5,3</td>
</tr>
</tbody>
</table>
### Semiconductors Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>thermal conductivity W/(cmK)</th>
<th>coefficient of thermal expansion $10^{-6}$/K</th>
<th>dielectric constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>1,5</td>
<td>2,5</td>
<td>11,8</td>
</tr>
<tr>
<td>Germanium</td>
<td>0,7</td>
<td>5,7</td>
<td>16,0</td>
</tr>
<tr>
<td>Gallium Arsenide</td>
<td>0,5</td>
<td>5,8</td>
<td>10,9</td>
</tr>
</tbody>
</table>

### Insulating Substrates Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>thermal conductivity W/(cmK)</th>
<th>coefficient of thermal expansion $10^{-6}$/K</th>
<th>dielectric constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon carbide SiC</td>
<td>2,2</td>
<td>3,7</td>
<td>42,0</td>
</tr>
<tr>
<td>Beryllia BeO</td>
<td>2,0</td>
<td>6,0</td>
<td>6,7</td>
</tr>
<tr>
<td>Alumina Al$_2$O$_3$</td>
<td>0,3</td>
<td>6,0</td>
<td>9,5</td>
</tr>
<tr>
<td>Silicon dioxide SiO$_2$</td>
<td>0,01</td>
<td>0,5</td>
<td>3,9</td>
</tr>
<tr>
<td>Polyimide</td>
<td>0,004</td>
<td></td>
<td>3,5</td>
</tr>
<tr>
<td>Epoxy glass (PC board)</td>
<td>0,003</td>
<td>15,0</td>
<td>5,0</td>
</tr>
</tbody>
</table>
IC Packages: Features

- The package should enable an optimal coupling of the die and its surrounding system

- Electrical coupling
  - Provide supply voltage and current
  - Adapt characteristic impedance of signals from die to board and vice versa

- Thermal coupling
  - Remove power dissipated by the IC

IC Packages: Issues

- Pin count
  - Today’s IC devices require 1000+ pins

- Mechanical stability
  - Due to large IC area
  - Due to high pin count

- High insertion force for sockets required
  - Due to high pin count
  - Use zero insertion force sockets
IC Packages: Issues

- Board manufacturing
  - Large pin count with very small grid

- Power dissipation
  - Todays high end ICs need to dissipate more than 50W

Packaging Process

1. Saw up the wafer into individual die.
2. Mount the die down onto a leadframe.
3. Wirebond from the die bond-pads to the leadframe.
4. Mold epoxy around the die to protect it.
5. Trim and form to break the individual packaged ICs apart.
6. Mark the packages.
Plastic Package Assembly Process

1. Wafer mounted on saw frame
2. Wafer sawn up on film frame
3. Pick off good die
4a. Dispense die attach epoxy
4b. Place die on the lead frame
5. Wirebond from die to frame
6. Mold
7. Trim and form

Source: ICKnowledge.com Introduction to IC Technology

Flip Chip Packaging

a) IC with array bond pads
b) IC after "bumping"
c) Mounted "flip chip" IC

Flip over the IC and solder down to the substrate

Source: ICKnowledge.com Introduction to IC Technology
IC Packages: Classification

- IC packages may be classified in different ways
  - Ceramic vs. Plastic
  - Through hole vs. surface mount
  - Pin count

Ceramic IC Packages

- Ceramic PGA: Pin Grid Array

CPGA
(Ceramic Pin Grid Array)

(bottom view)

Source: Intel Packaging Technology
Ceramic IC Packages

- Ceramic DIL: Dual In-Line
  
  **C-DIP**  
  (Ceramic Dual In-Line Package)  
  (Side-braze)

Source: Intel Packaging Technology

Ceramic IC Packages

- Ceramic LCC: Leadless Chip Carrier

  **LCC**  
  (Socket Mount)  
  (Bottom View)

Source: Intel Packaging Technology
Glass Sealed IC Packages

- Glass Sealed DIL with UV window

CERDIP
(Ceramic Dual In-Line Package)
(Insertion Mount; UV Window)

Source: Intel Packaging Technology

Plastic IC Packages

- Dual Row Plastic Packages

  Dual Row
  Small Outline Packages (SOP)

  PSOP
  (Plastic Small Outline Package)
  (Gull-Wing)

  SSOP
  (Shrink Small Outline Package)
  (Gull-Wing)

  SOJ
  (Small Outline Package)
  (J-Lead)

  TSOP
  (Thin Small Outline Package)
  (Gull-Wing)

Source: Intel Packaging Technology
Plastic IC Packages

- Quad Row Plastic Packages
  - PLCC (Plastic Leaded Chip Carrier)
  - PQFP (Plastic Quad Flatpack)
  - QFP (Quad Flatpack)
  - FLATPACK

Source: Intel Packaging Technology

Plastic IC Packages

- Plastic Ball Grid Arrays
  - PBGA / H-PBGA / HL-PBGA (Plastic Ball Grid Array)
  - MICRO BGA

Source: Intel Packaging Technology
Ball Grid Arrays

- Internal view

Plastic IC Packages

- Plastic Pin Grid Arrays

PPGA
(Plastic Pin Grid Array)

Source: Intel Packaging Technology
Flip Chip

- Minimize length of interconnection between chip and substrate
- Place solder bumps on the dice
- Flip chip over and align it with the contact pads on the substrate

Chip Carrier Packaging

✓ Chip carrier packaging is a platform upon which chips, passive components, device encapsulants, and thermal enhancement hardware are attached.
MCM – Multi Chip Modules

- MCMs have multiple chips connected to a single carrier.

- The carrier interconnects the chips and provides the external connections to the PCB.

Source: IBM Microelectronics

IC Packages

- Frequently used packages

Source: ICKnowledge.com Introduction to IC Technology
IO Standards

- While the package is the mechanical interface of an IC to its environment the IOs act as the electrical interface.

- There are different basic types of IO pads:
  - Input
  - Output
  - Bidirectional
  - Tri-State
  - Open collector/drain/emitter/source

IO Standards: Introduction

- There are multiple I/O standards in the area of high performance low voltage design.

- Required by the IC technology:
  - From 0.5 µm down one needs 3.3 V supply
  - From 0.25 µm down one needs 2.5 V supply
  - Further decreasing of device dimensions requires reduction of supply voltage.
    - To prevent break through of the field oxide
  - This requires new I/O standards for each new technology.
    - Many I/O standards define a power supply voltage.
IO Standards: Introduction

- Beside scaling down devices the system performance had to increase.

- We started with some MHz in the 80s and end now up with 1 GHz in the next year.
  - There is no longer a single IO specification that meets all requirements.

- New structures were needed to handle these frequencies.

IO Standards: Introduction

- These high frequencies limit system dimensions.

- These frequencies are no longer fed to just on one or two devices but across the whole board or rack.

- Reducing voltage swing increases system frequency
  - But reduces noise immunity

- Bus architectures had to be adapted to meet the performance goals.
IO Standards: Introduction

- Reduce bus dimensions
  - Bus length
  - Bus connectors

- Increase bus width

- Changing bus architecture changes the characteristic impedance of the bus.
  - New bus drivers were required

Motivations For New I/O Standards

- Reducing voltage swing

- Increasing bandwidth

- Adapting a standard for a well-defined local bus.
  - Defined driver, connector, dimensions, termination
  - Optimization of driver to the fixed bus topology possible
  - PCI bus
    - 33, 66, and 133 MHz for up to six connectors
  - AGP bus
    - for point-to-point connection
Motivations For New I/O Standards

- Using differential signaling for high speed board or system level interconnect.
  - To increase noise immunity.
  - Required for backplane interconnect.
  - When signals are lead across (multiple) connectors.

- Instead of defining a single I/O standard there is a special optimized standard for every topology.

Low Voltage I/O Standards

- Single Ended
  - LVTTL
  - LVCMOS
  - 2.5 V
  - 1.8V
  - 3.3 V PCI

- Differential
  - LVDS
  - LCPECL
  - LDT

- Voltage Referenced
  - AGP
  - CTT
  - GTL
  - HSTL I – IV
  - LVDCI
  - SSTL2
  - SSTL3
## Overview: Voltages

<table>
<thead>
<tr>
<th>Standard</th>
<th>Input Ref. Voltage</th>
<th>Output Supply Voltage</th>
<th>Board Term. Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVTTL</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>LVCMOS</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>LVPECL</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>1.8V</td>
<td>N/A</td>
<td>1.8</td>
<td>N/A</td>
</tr>
<tr>
<td>2.5V</td>
<td>N/A</td>
<td>2.5</td>
<td>N/A</td>
</tr>
<tr>
<td>3.3V PCI</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>LVDS</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>HSTL I</td>
<td>0.75</td>
<td>1.5</td>
<td>0.75</td>
</tr>
<tr>
<td>HSTL III</td>
<td>0.9</td>
<td>1.5</td>
<td>0.75</td>
</tr>
<tr>
<td>HSTL IV</td>
<td>0.9</td>
<td>1.5</td>
<td>0.75</td>
</tr>
<tr>
<td>GTL</td>
<td>0.8</td>
<td>N/A</td>
<td>1.2</td>
</tr>
<tr>
<td>GTL+</td>
<td>1.0</td>
<td>N/A</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL2</td>
<td>1.25</td>
<td>2.5</td>
<td>1.125</td>
</tr>
<tr>
<td>SSTL3</td>
<td>1.5</td>
<td>3.3</td>
<td>1.5</td>
</tr>
<tr>
<td>AGP</td>
<td>1.32</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>CTT</td>
<td>1.5</td>
<td>3.3</td>
<td>1.5</td>
</tr>
</tbody>
</table>
LVTTL / LVCMOS

- The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications.
  - It uses an LVTTL input buffer and a push-pull output buffer.

- The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5V applications.
  - It uses a 5V tolerant CMOS input buffer and a push-pull output buffer.

AGP

- The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications.
  - This standard requires a push-pull output buffer and a differential amplifier input buffer.
The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4).
- This standard requires a differential amplifier input buffer and a push-pull output buffer.

Applications:
- High-speed memories

The GTL - Gunning Transceiver Logic - standard is a high-speed bus standard (JESD8.3) invented by Xerox.
- This standard requires a differential amplifier input buffer and a Open Drain output buffer.

The GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

Applications
- High-speed processor interface
- High-speed backplane driver
The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6).

- This standard has four variations or classes.
- This standard requires a differential amplifier input buffer and a push-pull output buffer.

Applications
- High-speed memory interface to cache RAMs and fast SRAMs

HyperTransport technology is a new high-speed, high-performance point-to-point I/O standard for connecting integrated circuits on a motherboard.

- Formerly known as Lightning Data Transport, or LDT

- It is primarily targeted for the IT and telecommunication industries

- HyperTransport technology connections have two unidirectional point-to-point links with varied bit widths, and the clock is center-aligned with data.
LVDS

- LVDS is a low-voltage differential swing, general-purpose I/O standard.

- This I/O standard can transmit signals at high data rates across a variety of interconnect media such as:
  - Printed circuit board (PCB) traces
  - Backplanes
  - Cables

- with minimal power consumption and low noise.

LVDS

- IEEE 1596.3 and ANSI/TIA/EIA 644
- Defined up to 655 Mbit/s
- Power efficient
  - approx. 350 mV voltage swing
  - approx. 3.5 mA per channel, i.e. 1.2 mW
  - one tenth of PECL, 1/75 of RS-422
- Reduced common mode noise sensitivity
- Reduces power consumption of ECL based interconnect busses dramatically
- Simple termination
  - 100 Ω parallel resistor
LVDS Buffer Topology

Source: Altera Application Note AN 166
Xilinx Application XAPP 133

LVDS – A Design Example

- Serial-parallel converter at pin
- Converts data to slower clock frequency, 8-bit data
- Uses dedicated PLL
- Parallel-serial converter on output
LVPECL is another differential I/O standard.
- It requires two signal lines for transmitting one data bit.

This standard specifies two pins per input or output.

The voltage swing between these two signal lines is approximately 850 mV.

The LVPECL standard requires external resistor termination.
The LVPECL I/O standard is used in the fields of
- Telecommunications
- Data communications
- Clock distribution

LVPECL uses a positive power supply, and has relatively small voltage swing compared to TTL I/O standards,
- Thus LVPECL is suitable for high-speed systems.

Specified by PCI Special Interest Group (PCI-SIG)
- PCI standard 2.2
- 32/64 bit bus operating at 33 or 66 MHz
- Standard defines:
  - supply and output voltage
  - output current (V/I diagram)
  - device protection
  - bus dimensions
  - mechanics (connectors, boards, etc.)
- This is the standard for peripheral bus cards for PCs.
### SSTL2

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9).

- This standard has two classes, I and II.
- This standard requires a differential amplifier input buffer and an push-pull output buffer.

**Applications:**

- High-speed memory interfacing to SDRAMs 150 MHz

### SSTL3

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8).

- This standard has two classes, I and II.
- This standard requires a differential amplifier input buffer and an push-pull output buffer.

**Applications:**

- High-speed memory interfacing to SDRAMs 150 MHz
IO Termination

- Adapt the driver/receiver circuitry to the characteristic impedance of the trace on the board
- Avoid reflections on both the sender and receiver side
- There are different kinds of terminations used

Unterminated

- Driving Device
- Receiving Device
- $Z = 50$
- $V_{REF}$
Series Terminated Output

Driving Device

Receiving Device

Z = 50

Parallel Terminated Input

Driving Device

Receiving Device

Z = 50

V_{REF}

R_S

V_{TT}

R_{T2}

V_{REF}
Double Parallel Terminated

Driving Device

Receiving Device

\[ Z = 50 \]

General Termination

Driving Device

Receiving Device

\[ Z = 50 \]
I/O Standards Board Termination

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>$R_S$ (W)</th>
<th>$R_{T1}$ (W)</th>
<th>$R_{T2}$ (W)</th>
<th>$V_{REF}$ (V)</th>
<th>$V_{TT}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTL</td>
<td>–</td>
<td>50</td>
<td>50</td>
<td>0.8</td>
<td>1.2</td>
</tr>
<tr>
<td>GTL+</td>
<td>–</td>
<td>50</td>
<td>50</td>
<td>1.0</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL-2 Class I</td>
<td>25</td>
<td>–</td>
<td>50</td>
<td>1.25</td>
<td>1.25</td>
</tr>
<tr>
<td>SSTL-2 Class II</td>
<td>25</td>
<td>50</td>
<td>50</td>
<td>1.25</td>
<td>1.25</td>
</tr>
<tr>
<td>SSTL-3 Class I</td>
<td>25</td>
<td>–</td>
<td>50</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL-3 Class II</td>
<td>25</td>
<td>50</td>
<td>50</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>HSTL Class I</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>0.75</td>
<td>0.75</td>
</tr>
<tr>
<td>HSTL Class III</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>0.9</td>
<td>1.5</td>
</tr>
<tr>
<td>HSTL Class IV</td>
<td>–</td>
<td>50</td>
<td>50</td>
<td>0.9</td>
<td>1.5</td>
</tr>
<tr>
<td>AGP</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>1.32</td>
<td>–</td>
</tr>
<tr>
<td>CTT</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>LVDS</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>LVPECL</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

FPGAs meet I/O Requirements

- FPGAs operate typically on the interface of different systems and thus have to deal with multiple I/O standards.
- Todays FPGAs offer support for multiple I/O standards.
- One can mix up several I/O standards even within one device.
FPGAs meet I/O Requirements

- Power supply of the devices is split into a core supply and a peripheral supply.
  - They are connected separately to different voltages.

- I/Os of FPGAs are grouped to several "I/O banks"

- Each I/O bank has its separate peripheral supply.
  - Consult the datasheet of the respective device to get the number of banks and the I/O standards supported.

FPGAs meet I/O Requirements

- Depending on the requirements for reference, output, and termination voltage one has to group its I/Os.
  - Select the I/O signals in your design with the same requirements and put them in the same I/O bank.
  - Differential I/O require of course two adjacent pins.
  - Differential I/O is usually somewhat limited.
Example: APEX 20KE I/O Banks

- Regular I/O Blocks
- Support:
  - AGP
  - CTT
  - GTL+
  - HSTL Class I, II, III, IV
  - LVCMOS
  - LVTTL
  - 3.3-V PCI
  - SSTL-2 Class I and II
  - SSTL-3 Class I and II

Summary

- We learned in this lecture about
  - IC packaging – why and how
  - Frequently used IC packages
  - Low voltge IO standards