Energy Efficient High Speed On-Chip Signaling in Deep Submicron CMOS Technology

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Outlines

- Design challenges in Deep-submicron CMOS
- Our Approach to tackle DSM effects
- Problem formulation and Related work
- Current mode MVL
  - Qualitative analysis of the On-Chip Interconnect (OCI)
  - Energy-efficient signaling
- Simulation results
- Concluding remarks
DSM: opportunities and challenges

<table>
<thead>
<tr>
<th>L (µm)</th>
<th>Tox (Å)</th>
<th>Vdd (in V)</th>
<th>Vt (in V)</th>
<th>Line thickness (µm)</th>
<th>Width and spacing (µm)</th>
<th>Sheet resistance (Ω/ )</th>
<th>Tins (in µm)</th>
<th>Dielectric constant</th>
</tr>
</thead>
<tbody>
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<td>0.3</td>
<td>0.044</td>
<td>0.65</td>
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<td>0.048</td>
<td>0.5</td>
<td>2.7</td>
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<td>0.065</td>
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<td>2.3</td>
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<td>0.2</td>
<td>0.1</td>
<td>0.11</td>
<td>0.27</td>
<td>1.8</td>
</tr>
</tbody>
</table>

Contd., Main Disadvantages

- Static power is increasing
- Increase of the digital noise
- Reduced drive current, \[ I \approx C_{ox} W V_{sat} (V_{dd}-V_{t}) \]
- Delay and power caused by the interconnect is getting more dominant
- Increased design-complexity
Our approach to tackle DSM effects

How can I get around DSM effects to achieve GSI without using expensive or special process?

Use a **signaling scheme** that is **robust against DSM noise** and allows for **low-power, high-speed** communication between digital blocks!
On-chip signaling in DSM

Is there a clever way to model the VLSI circuit?
Problem formulation

Can we use information theory to understand/solve our problem?

Information *can be transmitted* through a **noisy channel** at a rate nearly equal to the **channel capacity** ($\phi$)

**Shannon theorem (1948)**

$\phi \equiv \log_2(1 + P/(BN_0))$, $B$: bandwidth, $P$: symbol power, $N_0$: PSD of the AWGN
Let $\gamma_{ij} = \text{Watts}/R_{ij}$, the quantity that measures the power efficiency.
For each communication from $j$ to $i$ at a rate $R_{ij}$, our objective is to solve
the following optimization problem.

Minimize $\gamma_{ij}$ subject to
1) The achievable data-rate, from $j$ to $i$, is equal to $R_{ij}$
2) Bit-Error-Rate, $BER_{ij} \leq \tau$
Our solution to solve \textit{OPT}
Related work

- Most reported techniques are based on reduced-voltage swing signaling with repeaters insertion.

On-chip interconnect (in DSM)

\[ \text{Cin1-in2: Coupling capacitance between aggressor and victim} \]
Modeling of the OCI

In our experiments, $L$ and $C$ were obtained using LINPAR (Matrix Parameters for Multiconductor Transmission Lines).

Resistance

$\rho$: resistivity

$R \equiv \begin{cases} 
\frac{\rho}{(w \times h)} & \text{if } 0 \leq f \leq f_\delta \\
\left(\sqrt{f \times \pi \times \mu \times \rho}\right)/(w \times 2) & \text{if } f > f_\delta 
\end{cases}$

$\delta$ depth, $f_\delta$

$f_\delta \approx \frac{\rho}{\pi \times \mu \times w^2}$
Capacity of the OCI

\[ \zeta(L, R, C, d) = C d^2 \sqrt{(R^2 C d^2 - 2L^2)^2 + 2.25L^2 d^2} \]

\[ \Delta(L, R, C, d) = 2LCd^2 - (RC)^2 d^4 + \zeta(L, R, C, d) \]

\[ B_2 = \frac{\sqrt{\Delta(L, R, C, d)}}{2.83\pi LCd^2} \]

\[ \beta = 0.5(1 + \text{sign}(B_2 - f_\delta)) \]

\[ B = \beta \left[ \frac{0.56w^2}{\pi^3 d^4 \pi \mu C^2} \right]^{1/3} + (1 - \beta)B_2 \]
Shannon-Capacity of the OCI

\[ \phi = \log_2(1 + \frac{P}{BN_0}), \quad B: \text{bandwidth, } P: \text{symbol power, } N_0: \text{PSD of the AWGN} \]

\(N_0\) is a function of:

1) Fundamental noise
2) Cross-talk noise
3) Power-supply noise
4) Leakage noise,
5) Charge-sharing noise
etc...

Upper-limit: \[ \phi = \log_2(1 + \frac{P}{BKT}) \],

\(K\): Boltzmann’s constant, \(T\): Device temperature
Voltage mode CMOS: Binary techniques

\[ s(t) = \sum_{n=0}^{\infty} a_n \times h_T(t-nT) \]
Generalization: Multi-valued voltage mode

Given $V_{dd}$, $V_{ss}$ and $M$. What is the BER of my circuit?

$$P_f = \frac{2(M-1)}{M \log(M)} Q\left(\sqrt{\frac{T d V_{dd}^2 \log(M)}}{(M-1)^2 N_0}\right)$$

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-\frac{t^2}{2}} dt$$
Why do we need to use higher values of $M$?

\[ R_b = 2 \log(M) \left[ B = \beta \left( \frac{0.56w^2}{\pi^3d^4\pi\mu C^2} \right)^{1/3} + (1 - \beta)B_2 \right] \]
Robust signaling (current vers. Voltage mode)

- Robust against power supply noise
- It has lower $\gamma_{ij}$
- Easy to generate multiple current sources without the need for DC-converters
- Better noise immunity
- Lower delay
- Widely used for off-chip signaling
- But …. Mixed signal design

Ref, W. J. Dally et al, ”Digital Systems Engineering”, Cambridge univ. press
Scenarios for high-speed signaling

On-chip interconnect of length $d$ having a bandwidth $B$

*Binary signaling (2-CMVL)*

OR

*M-CMVL*

$\gamma_{b,d} = K\gamma_b$
E-VIJIM algorithm

For a given $N_0$, $T_b$, $d$, $w$, $M_{max}$, $I$, $p$, $w$, $h$, $s$, $R_d$, $L$ and $C$

$s=<>; /* The solution is initialized to NULL */$
compute $B$
$M=2$, compute $R_d$ denote this by $R_b$
if ($R_b<= R_d$)
    Compute $d_{min}$ by setting $R_d=R_b$
    Compute $K$ (number of regenerative repeaters)
    for $k=1:K$
        Compute $I_{max}$
        Compute $\gamma_{d,b}$
        Save the results to $s$
        Goto end-E-VIJIM
    Compute $M$
    Compute $I_{max}$ and save the results to $s$
    Goto end-E-VIJIM
else
    compute $I_{max}$ save the results to $s$
end E-VIJIM:
Select the minimum solution from $S$. If the value of $I_{max}$ is more than $I$ then print an error.
### Experimental results (Metal-2)

<table>
<thead>
<tr>
<th>conf.</th>
<th>w(μm)</th>
<th>h(μm)</th>
<th>s(μm)</th>
<th>L(H/m)</th>
<th>C(F/m)</th>
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</thead>
<tbody>
<tr>
<td>CF1</td>
<td>0.13</td>
<td>0.26</td>
<td>0.13</td>
<td>3.30E-07</td>
<td>1.56E-10</td>
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<td>CF2</td>
<td>0.86</td>
<td>1.72</td>
<td>0.86</td>
<td>1.92E-07</td>
<td>2.40E-10</td>
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</table>

<table>
<thead>
<tr>
<th>d (mm)</th>
<th>fmaxh(GHz)</th>
<th>fmax(GHz)</th>
<th>error</th>
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<tbody>
<tr>
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<td>250</td>
<td>248.3</td>
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<td>0.2</td>
<td>50</td>
<td>48.24</td>
<td>3.64%</td>
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<tr>
<td>0.4</td>
<td>11</td>
<td>10</td>
<td>10%</td>
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<tr>
<td>0.5</td>
<td>6.4</td>
<td>6.29</td>
<td>1.74%</td>
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<td>4.4</td>
<td>4.32</td>
<td>1.85%</td>
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<tr>
<td>0.7</td>
<td>3.2</td>
<td>3.15</td>
<td>1.58%</td>
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<td>0.8</td>
<td>2.5</td>
<td>2.4</td>
<td>4.16%</td>
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<td>1</td>
<td>1.59</td>
<td>1.53</td>
<td>3.92%</td>
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<td>0.3</td>
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<tr>
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<td>0.16</td>
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<tr>
<td>8</td>
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<tr>
<td>d (mm)</td>
<td>fmaxh(GHz)</td>
<td>fmax(GHz)</td>
<td>error</td>
</tr>
<tr>
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<td>0.1</td>
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<td>1</td>
<td>1</td>
<td>0%</td>
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<td>0.73</td>
<td>0.74</td>
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<tr>
<td>9</td>
<td>0.56</td>
<td>0.57</td>
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<tr>
<td>10</td>
<td>0.43</td>
<td>0.46</td>
<td>7%</td>
</tr>
</tbody>
</table>
$d \leq 1.2\text{mm}$, 2-MVL is the optimum.

$d=4\text{mm}$, 4-CMVL is the opt. at 16GHz

$d=5.5\text{mm}$, for $600\text{MHz} > 5.33\text{GHz}$, 2-CMVL is the opt. From $5.33 > 8\text{GHz}$, 4-CMVL is the opt.
Concluding remarks

- Techniques for using M-CMVL current mode energy efficient high-speed signaling over on-chip interconnect were presented.

- An analogy between on-chip signaling and digital communication over band-limited channel was reported.

- A algorithm for computing channel capacity of the on-chip interconnect was derived. Our algorithm has an average error less than 10%.

- A pseudo-code for fast searching of the energy efficient signaling was derived.
• Implementation of E-VIJIM shows that up to two times improvement in power can be achieved if four current levels are used for on-chip signaling.

• Over 1.4 times area-improvement has been achieved.

• Bottleneck: Mixed Signal Design

4-CMVL is the most promising candidate for signaling over long-on chip interconnect.

Currently, encoder-decoder is being implemented. The results will be submitted to the special issue of “on-chip signaling in DSM”, Journal of Analog Integ. Circ. And Sig. Process.