Stochastic Power/Ground Supply Voltage Prediction and Optimization Via Analytical Placement

Andrew B. Kahng, *Member, IEEE*, Bao Liu, *Member, IEEE*, and Qinke Wang

***Abstract*—Increasingly significant power/ground (P/G) supply voltage degradation in nanometer VLSI designs leads to system performance degradation and even malfunction, which requires stochastic analysis and optimization techniques. We represent the supply voltage degradation at a P/G node as a function of the supply currents and the effective resistance of a P/G supply network and propose an efficient stochastic system-level P/G supply voltage prediction method, which computes P/G supply network effective resistances in a random walk process. We further propose to reduce P/G supply voltage degradation via placement of supply current sources, and integrate P/G supply voltage degradation reduction with conventional placement objectives in an analytical placement framework. Our experimental results show that the proposed stochastic P/G supply network prediction method achieves 10×–100× speedup compared with traditional SPICE simulation, and the proposed P/G supply voltage degradation aware placement achieves an average of 20.9% (11.7%) reduction on maximum (average) supply voltage degradation with only 4.3% wirelength increase.**

***Index Terms*—Analytical placement, infrared (IR) drop analysis, power/ground (P/G) distribution, VLSI design.**

I. Introduction

VLSI technology scaling has introduced increasingly significant supply voltage degradation along the power/ground (P/G) supply networks, e.g., power supply voltage drop and ground supply voltage bounce, in a nanometer VLSI design. The reasons are multifold: 1) shrinking layout feature sizes lead to increased interconnect resistance; 2) increasing device density leads to increased supply current; and 3) higher clock frequency leads to more significant inductance effect which brings additional supply voltage drop. On the other hand, P/G supply voltage scaling implies a shrinking noise margin for a transistor. Supply voltage degradation which exceeds the noise margin would result in logic malfunction. Less severe supply voltage degradation still leads to transistor and even system performance degradation. A 10% supply voltage degradation could be responsible for 10% transistor performance degradation and the effect is super-linear [26]. Consequently, nanometer VLSI system design needs to achieve signal integrity for the P/G supply voltages.

A P/G supply network can be modeled as a distributed *RLC* netlist, and conventional interconnect model order reduction [20], [21], and analysis techniques [23], [30] are applicable for P/G networks. However, significant challenges in efficiency and scalability improvement are present for P/G network analysis due to the nontree topology, the large instance size, and the large numbers of excitation and observation nodes of a P/G network. Special P/G network analysis techniques which aim for scalability and efficiency improvement include random walk [23], multigrid-like [17], [18], and hierarchical [29] approaches.

P/G supply voltages depend on the underlying stochastic circuit switching activity, which are correlated and time-varying [2]. As technology scales, increased process variations result in increased variations in terms of interconnect resistance, inductance, capacitance, and of P/G supply voltages. Traditional best/worst corner-based analysis method cannot provide accurate estimates and stochastic methods must be applied for nanometer P/G supply voltage analysis [3].

Random walk has been an efficient technique in solving a stochastic process, for example, in Schödinger's equation in nanometer simulation. Top-down approaches, such as multigrid-like [17], [18], hierarchical [29], and partition-based [16] approaches, which improve P/G supply network analysis scalability by combining efficiency on higher hierarchy levels with accuracy on finer hierarchy levels based on global abstraction of a P/G supply network. Random walk techniques compute dc responses [23] or frequency domain response moments [12] by exploiting locality of supply voltage degradation, which says that supply voltage drop of a P/G node is largely determined by its neighboring region, e.g., from the node to a nearby P/G supply pad. As a result, the time complexity of a random walk process depends on the expected distance from an observation node to a P/G node of known voltages, such as a P/G supply pad, and is independent of the size of the entire P/G supply network.

P/G supply voltage degradation includes three components: 1) dc supply voltage degradation, i.e., infrared (IR) drop, which is observed when a P/G supply network is modeled as a resistive network with dc supply current sources; 2) ac supply voltage degradation, which appears in an *RC* P/G network with ac supply current sources; and 3) LdI/dt supply voltage degradation which is due to inductive effect. To reduce these supply voltage degradation components, techniques include the following:

1) wiresizing or edge augmentation of a P/G network for reduced interconnect resistance or supply current along a supply current path;
2) adding large decoupling capacitors close to supply voltage degradation hot spots, which serve as "charge reservoirs"

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and form shortcut supply current paths (hence reduce supply voltage drop). For high frequency designs, a number of decoupling capacitors need to be added at different P/G network hierarchy levels to cancel inductance effect and lower P/G network resistances over a wide range of frequency [22];

3) circuit detuning for reduced simultaneous supply current;
4) placement or P/G supply pad allocation [28] which moves large supply current modules closer to P/G supply pads or to be more evenly distributed.

Certain placement and floorplanning related techniques have been proposed for supply voltage reduction. Local placement adjustment helps decoupling capacitor insertion which is limited by available empty space in a placement [25], [31]. Mixed integer linear programming is proposed for finding the locations of P/G supply pads [28]. Network flow is proposed for P/G supply network construction and supply voltage degradation is included in a floorplan objective [6]. However, to the best of our knowledge, no supply voltage degradation reduction placement technique is presented.

In this paper, we propose an analytical placement method for P/G supply voltage integrity, based on a stochastic P/G supply voltage prediction method via random walk process. Our contributions are as follows.

1) We represent supply voltage degradation at a P/G node as a function of supply currents effective resistances in a P/G network. For P/G supply voltage degradation analysis, we apply random walk, graph contraction, and interpolation techniques for efficiency improvement in finding effective resistances.
2) We present greedy algorithms which achieve optimum placement with minimized supply voltage degradation at a given node or minimized total supply voltage degradation over all P/G nodes. It is NP-hard to find a placement which minimizes maximum supply voltage degradation.
3) We propose supply voltage degradation aware placement by integrating the supply voltage degradation metric in an analytical placement objective via a smooth approximation function that enables differentiation of the maximum function.

We evaluate our method on two industry designs in terms of voltage degradation, placed wirelength and runtime. Our experimental results show that the proposed stochastic P/G supply network prediction method achieves $10\times$–$100\times$ speedup compared with traditional SPICE simulation, and the proposed P/G supply voltage degradation reduction by analytical placement achieves an average of 20.9% (11.7%) reduction of maximum (average) supply voltage degradation with only 4.3% wirelength increase.

The rest of this paper is organized as follows. We introduce motivations and problem formulation in Section II and present random walk-based stochastic system-level P/G supply voltage prediction method in Section III. We present theoretical analysis on placement for supply voltage drop reduction in Section IV and introduce an analytical placer and its integration with supply voltage drop reduction in Section V. Our experimental results are presented in Section VI, and we conclude in Section VII.

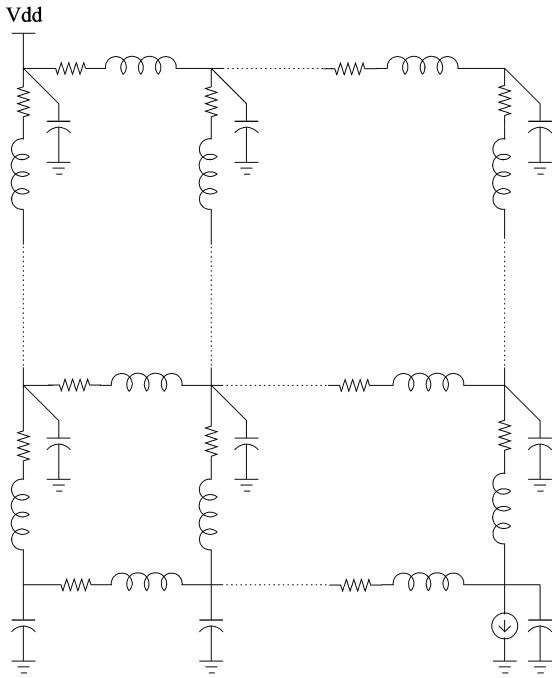

Fig. 1. Power supply grid with a resistor and an inductor on each segment and a ground capacitor and a possible voltage/current source at each node.

II. Problem Formulation

A P/G supply network connects P/G supply sources (pads) to active devices which draw supply currents as signal transitions occur, and cause supply voltage degradation at active devices, due to the inherent resistance and inductance of the P/G supply network. We model a P/G supply network as an *RLC* interconnect (see Fig. 1), with P/G sources modeled as dc voltage sources and active devices modeled as time-varying current sources which inject worst case supply currents (e.g., "maximum current envelopes" [4]). Such a worst case supply current waveform comes from simulation [1], a special tool [4], or static timing analysis (e.g., through worst case slew rate and arrival "timing window" report).

For system level prediction of P/G supply voltage in a million-gate VLSI design subject to process, environmental, and stochastic circuit switching activity variations, we propose stochastic P/G supply voltage prediction via a random walk process. We formulate the P/G supply network analysis problem as follows.

Problem 1 (P/G Supply Voltage Prediction): Given the following, find the voltages of a subset of observation nodes

1) *RLC*(K) netlist of a P/G supply network;
2) subset of nodes with DC supply voltage sources;
3) subset of nodes with supply current sources.

Existing supply voltage drop reduction techniques focus on optimization of P/G supply network designs, for example, by wiresizing, edge augmentation, and decoupling capacitor insertion. However, supply voltage degradation occurs not only due to poor P/G supply network design, but also due to unexpected large supply currents at specific time steps and specific locations, which suggests application of circuit design and placement techniques for supply voltage degradation reduction. For

example, circuit detuning spreads the supply currents in the time domain to reduce the maximum supply current at a particular time step.

We propose supply voltage degradation reduction via placement of supply current sources, without significant compromise of conventional placement objectives such as wirelength, area, and performance.

Problem 2 (P/G Supply Voltage Placement Optimization): Given the following:

1) *RLC*(K) netlist of a P/G supply network;
2) subset of nodes with DC supply voltage sources;
3) a set of supply current sources;

find a mapping between the supply current sources and the P/G supply network nodes such that:

a) the maximum;
b) the sum; or
c) one of the P/G supply voltage degradations is minimized, without significant degradation in conventional placement objectives such as wirelength, area, and timing.

We adopt the following notations in this paper.

G	conductance matrix;
V	node voltage vector;
I	source current vector;
(p, q)	edge between nodes p and q;
E	set of edges in a P/G network;
T_p	subtree which is rooted at node p;
$P(p, q)$	path between nodes p and q in a tree;
G_{pq}	conductance between nodes p and q;
I_q	supply current at node q;
V_q	supply current at node q;
$\Delta V(q)$	supply voltage degradation at node q;
$Z(p, q)$	effective impedance between nodes p and q.

III. Stochastic P/G Supply Voltage Prediction

A. Random Walk in a P/G Network

P/G network analysis can be performed by straightforward circuit nodal analysis, e.g., via a direct equation system solver, as follows [23], [30]:

$$\begin{aligned} Gx + C\dot{x} &= Bu \\ x &= (I + sG^{-1}C)^{-1}G^{-1}Bu \end{aligned} \tag{1}$$

where G is the conductance matrix, C is the capacitance matrix, u is the external voltage source vector, x is the unknown voltage or current vector, $\dot{x}$ is the time domain derivative of x, I is unit matrix, and B is the adjacency matrix associated with the external voltage sources.

As we can see, such a direct solver suffers efficiency and scalability problems, for example, in computing the inverse of a matrix G^{-1}. A more efficient approach is to apply Monte Carlo methods of partial differential equations (PDEs), e.g., random walk [10].

For example, in a purely resistive P/G network (e.g., Fig. 1 with zero capacitances and inductances), for a node q, with conductance G_{pq} between q and each of its neighboring node p, and a current source I_q between q and the ground, Kirchoff's current law gives the ground current I_q and voltage V_q of node q as follows:

$$V_q = \frac{\sum_{(p,q)\in E} G_{pq}V_p - I_q}{\sum_{(p,q)\in E} G_{pq}}. \tag{2}$$

This is the finite-difference form of a boundary value problem of partial differential equations, where each node voltage is associated with neighboring node voltages and the known node voltages consist of the boundary conditions [17], e.g., in a continuous resistive surface, (2) becomes Poission's equation

$$I_q(x, y) = \frac{\partial^2 G(x, y)V(x, y)}{\partial x^2} + \frac{\partial^2 G(x, y)V(x, y)}{\partial y^2} \tag{3}$$

where $I_q(x, y)$, $G(x, y)$, and $V(x, y)$ are ground current, conductance, and voltage at point (x, y), respectively.

One of the Monte Carlo methods of solving PDEs, i.e., random walk, is explained in [23] as follows (Algorithm 2). A traveler pays an amount $A(q) = \left(I_q/\sum_{(p,q)\in E} G_{pq}\right)$ (e.g., for lodging) at a node q, with a probability $\mathrm{Prob}(p, q) = \left(G_{pq}/\sum_{(p,q)\in E} G_{pq}\right)$ of going to an adjacent node p, until he reaches a node of V_{dd} voltage source (home), where he stays and receives a reward (which equals the V_{dd} voltage). The average net gain (the reward minus the costs) of the trip approaches the voltage at node q. Such a random walk game avoids prohibitive full scale analysis and exploits locality of the problem (since most of the traversals are at neighboring nodes).

Because of the locality of the process, which states that most of the traversals are in a neighboring region between the observation node and a node of known voltage such as a power pad, the time complexity of such a random walk process depends on the expected distance from the observation node to the nodes of known voltages, and is independent on the size of the entire P/G supply network. As a result, random walk is very efficient in computing nodal voltages at specific locations, is suitable for parallel processing, and can be implemented in a hierarchical P/G supply network analysis scheme, e.g., to compute the nodal voltages for the hierarchical boundaries to enable P/G supply network partition and hierarchical analysis.

Algorithm 1: Random Walk in a Resistive Network

Input: Resistive netlist, boundary nodes with known voltages
Output: Voltage of the observation node

1. Starting from the observation node
2. While (not reaching a boundary node)
3. Pay $A(q)$ at node q
4. Walk to an adjacent node p with $\mathrm{Prob}(p, q)$
5. Gain V_b of the voltage at boundary node b
6. Return the net gain

B. Finding Effective Resistance Via Random Walk

A VLSI P/G supply network modeled as an *RLC* network is a linear system, where the nodal voltages are summation of contributions of the supply currents

$$\Delta V(q) = \sum_{p} Z(p,q) I_p \tag{4}$$

where $Z(p,q)$ is the effective impedance for a current source at node p to inject a noise voltage at node q.

We propose to compute $Z(p,q)$ by a random walk process as follows. An effective impedance $Z(p,q)$ is given by the voltage at node q when the P/G network is driven by a single unit source current at node p. If we construct two random walk paths that respectively start from nodes p and q and end at a supply pad, then $Z(p,q)$ is given by the resistance of the common part of the two paths, as in a tree-structure supply network. A random walk path is generated with the following transition probability from node p to node q:

$$\text{Prob}(p,q) = \frac{G_{p,q}}{\sum_{(p,k)\in E} G_{p,k}} \tag{5}$$

so that a random walk path follows the corresponding current distribution probability. Averaging over a large number of probabilistic instances gives increased accuracy.

Algorithm 2: Random Walk Effective Impedance Computation

Input: P/G network, boundary nodes with known voltages
Output: Effective impedance $Z(p,q)$ between nodes p and q

1. Apply Algorithm 1 and find a random walk path $P(p,b)$ from node p to a boundary node b
2. Apply Algorithm 1 and find a random walk path $P(q,d)$ from node q to a boundary node d
3. Return the impedance of the common part of the paths $P(p,b) \cap P(q,d)$.

For scalability and efficiency improvement, we also apply multigrid and interpolation techniques. We contract a P/G netlist by merging nodes and computing parallel resistances. Resistances are computed directly for a subset of the nodes, while resistances at the other nodes are computed by interpolation. Note that interpolation is applicable for resistance computation, because the effective resistance of a node is bounded by those of its neighboring nodes, even though its voltage may not be bounded by those of its neighboring nodes.

IV. Placement for P/G Supply Voltage Integrity

In this section, we present supply voltage degradation as a function of supply currents, and study the problem of locating the supply current sources (cells) to minimize supply voltage degradation. We present greedy algorithms which achieve optimum placement with minimized total supply voltage degradation over all P/G nodes or minimized supply voltage degradation at a given P/G node, and demonstrate that it is NP-hard to achieve a placement with minimized maximum supply voltage degradation. We integrate the proposed supply voltage degradation metric in an analytic placement objective in Section V.

A. P/G Network in a Tree Structure

For a given resistive tree-structure P/G supply network with dc supply current sources at each node, finding supply voltage degradation resembles Elmore delay calculation, i.e., by replacing ground capacitances by current sources

$$\begin{aligned}\Delta V(q) &= \sum_{(i,j)\in P(s,q)} R_{ij} \left(\sum_{p\in T_j} I_p \right) \\ &= \sum_{p\in T_s} R(p,q) I_p \\ Z(p,q) &= \sum_{(i,j)\in P(s,q)\cap P(s,p)} R_{ij}\end{aligned} \tag{6}$$

where a P/G supply pad s is the root of the P/G supply tree, $P(s,q)$ is the path in the tree between node s and node q, each edge (i,j) has a resistance of R_{ij}, each node has a supply current of I_p, and T_j is the subtree rooted at node j.

Problem 3: For a given resistive tree-structure P/G supply network, locate the dc supply current sources, such that:

a) maximum supply voltage drop;
b) total supply voltage drop; or
c) supply voltage drop at a given node is minimized.

Observation 1: The minimized maximum supply voltage drop placement [Problem 2(a)] with a tree-structure P/G network keeps a partial ordering, such that a node has current no larger than that of its parent node

$$i \in T_j \Rightarrow I_i \le I_j. \tag{7}$$

For the case of a single P/G supply line, the optimal placement strategy is to greedily locate the largest supply current source closest to the P/G supply source. In the presence of a branch in the P/G network, optimal placement implies a partition, i.e., to partition supply current sources I_q into two sets, with weights of path resistance $\sum_{(i,j)\in P(s,q)} R_{ij}$ from the source s to each child node q of the branching point, which is NP-hard.

Observation 2: It is NP-hard to find a placement which minimizes the maximum voltage degradation in a tree-structure P/G supply network [Problem 2(a)].

B. P/G Network in a General Structure

In a general-structure P/G network which is a linear system, a nodal voltage is given by the summation of the contributions of each current source k as is given by (4).

Problem 4: For a given P/G supply network, locate the supply current sources such that:

a) maximum supply voltage drop;
b) total supply voltage drop; or
c) supply voltage drop at a given node is minimized.

We propose two greedy algorithms for assigning effective impedances to current sources to optimize the total supply voltage degradation or the supply voltage degradation at a given P/G network node.

Observation 3: The optimum placement which minimizes the total supply voltage drop in a P/G supply network [Problem

3(b)] is given by a greedy algorithm, which locates a large current I_p to have a small impedance $\sum_q Z(p,q)$.

Observation 4: The optimum placement which minimizes the voltage drop at a given node q in a P/G supply network [Problem 3(c)] is given by a greedy algorithm, which locates a large current I_p to have a small impedance $Z(p,q)$.

V. Supply Voltage Integrity Aware Analytical Placement

In this section, we include supply voltage integrity in the objective of an analytical placement framework. Analytical placement has been developed as one of the dominant VLSI placement techniques of today, due to its excellent solution quality and its high extensibility to optimize a variety of design objectives which emerge in nanometer VLSI design [13], [19]. We observe that analytical placement is the only VLSI placement method which is capable of optimizing supply voltage integrity accurately.

A. Basic Analytical Placement

Analytical placement applies the approximation/relaxation method in global optimization to VLSI placement and transforms the original NP-hard problem to a continuous (near-convex) optimization problem and applies continuous optimization techniques such as conjugate gradient method to achieve a close approximation of the global optimum solution. The basis of analytical placement is the smooth approximation functions for the placement objectives and constraints. For example [13], the half-perimeter wirelength of a net n with k terminals $(x_1,y_1),\ldots,(x_k,y_k)$ in a Manhattan plane is given by

$$l(n) = \mathrm{Max}_i(x_i) - \mathrm{Min}_i(x_i) + \mathrm{Max}_i(y_i) - \mathrm{Min}_i(y_i) \quad (8)$$

and is approximated by

$$l(n) = \alpha\left(\log\left(\sum_i e^{x_i/\alpha}\right) + \log\left(\sum_i e^{-x_i/\alpha}\right) + \log\left(\sum_i e^{y_i/\alpha}\right) + \log\left(\sum_i e^{-y_i/\alpha}\right)\right). \quad (9)$$

A component c of rectangle (x_1,y_1,x_2,y_2) has contribution to layout density at location (x,y) of

$$d(c,x,y) = \begin{cases} 1, & (x_1 < x < x_2,\ y_1 < y < y_2) \\ 0, & \text{otherwise} \end{cases} \quad (10)$$

and is approximated by

$$d(c,x,y) = b\left(x - \frac{x_2+x_1}{2}, x_2 - x_1\right) \cdot b\left(y - \frac{y_2+y_1}{2}, y_2 - y_1\right) \quad (11)$$

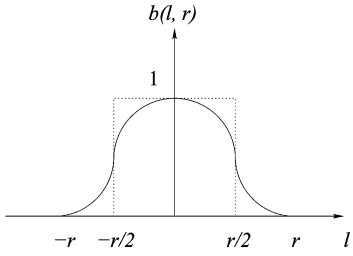

Fig. 2. Bell-shaped function $b(l,r)$ (in solid curves) which approximates the pulse function (in dotted lines) of width r and height 1. The areas under the bell-shaped function and the pulse function are equal.

where $b(l,r)$ is a bell-shaped function (see Fig. 2)

$$b(l,r) = \begin{cases} \frac{1-2l^2}{r^2} & \left(\frac{0<l<r}{2}\right) \\ \frac{2(l-r)^2}{r^2} & \left(\frac{r}{2} < l < r\right) \end{cases}. \quad (12)$$

With these smooth and differentiable approximation functions for the placement objectives and constraints, analytical placement optimize the following objective [13]:

$$\text{minimize} \sum_{n\in N} l(n) + \frac{1}{\beta}\sum_{(x,y)\in G}(D(x,y) - \bar{D})^2 \quad (13)$$

where

$$D(x,y) = \sum_{c\in C} d(c,x,y)$$
$$\bar{D} = \sum_{(x,y)\in G} \frac{D(x,y)}{(m\cdot n)}. \quad (14)$$

G is an $m \times n$ grid of layout density sampling points and β is a weighting factor which balances wirelength minimization and cell density deviation minimization.

Note that the approximated problem is not a convex optimization problem, because the bell-shaped function (12) is not convex, analytical placement does not guarantee to achieve global optimum. To achieve a close approximation of the global optimum solution, analytical placement applies a recursive relaxation technique, starting with almost convex approximation of cell densities with a large r in (12) and a small number of sampling points in G, and proceeds towards increasingly accurate approximation by recursively scaling down r and the distance between sampling points in G. For each r and G, the weighting factor β also scales down recursively, such that the placement starts with minimum wirelength and congested components to solutions with more evenly distributed components.

B. Supply Voltage Integrity Aware Analytical Placement

We now propose smooth functions for average and maximum supply voltage degradation evaluation and their integration in an analytical placement objective.

1) Average Supply Voltage Degradation: For N observation nodes in a P/G supply network, the average supply voltage degradation is given by

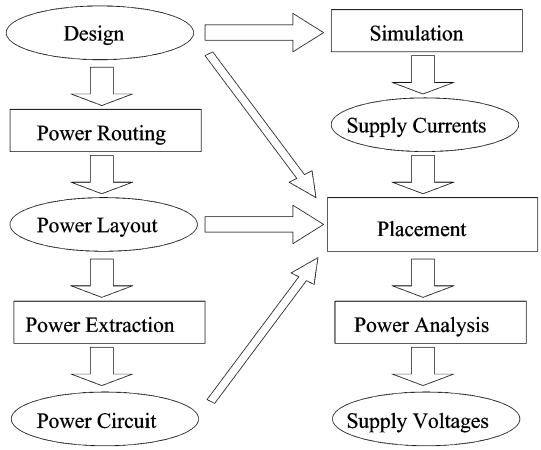

Fig. 3. Flow for evaluating voltage-degradation-aware placement techniques.

$$\Delta V_{\text{avg}} = \frac{1}{N} \sum_{p} \sum_{q} Z(p,q) I_p. \tag{15}$$

For efficiency improvement, we compute effective impedances $Z(p,q)$ for a subset of P/G nodes (for example, the observation nodes); and apply bilinear interpolation to obtain effective impedance at continuous locations.

2) Maximum Supply Voltage Degradation: Maximum supply voltage degradation over all P/G network nodes is given as follows:

$$\Delta V_{\max} = \max_{q} \{\Delta V(q)\}. \tag{16}$$

However, the $\max$ function in (16) cannot be efficiently minimized using nonlinear optimization techniques, since it is not smooth or differentiable. We apply a **log-sum-exp** method to capture the maximum supply voltage degradation while simultaneously obtaining the desirable characteristic of continuous differentiability

$$\Delta V_{\max} = \alpha \cdot \ln \left(\sum_{q} e^{\Delta V_q / \alpha} \right) \tag{17}$$

where α is a smoothing parameter: $\Delta V_{\max}$ is strictly convex, continuously differentiable and converges to the maximum supply voltage degradation as α converges to 0. The log-sum-exp formula picks the maximum voltage degradation among the voltage degradation of all the power nodes; it has been previously used in physical design applications such as transistor sizing and wirelength-driven placement [5], [13], [24].

Intuitively, the smoothing parameter α in (17) can also be regarded as a "significance criterion" for choosing P/G network nodes with large voltage degradation to minimize. Only power nodes with a voltage degradation which has a small difference from the maximum voltage degradation relative to α will introduce significant differentials of module locations, as shown in the following equation:

$$\frac{\partial \Delta V_{\max}}{\partial V_q} = \frac{1}{\sum\limits_{p} e^{(V_p - V_q)/\alpha}}. \tag{18}$$

In the experiments, we set α to one-tenth of the maximum voltage degradation.

3) Implementation: We combine supply voltage degradation with existing placement metrics, e.g., wirelength, congestion, and timing, in an analytical placer. For example, combining wirelength and supply voltage degradation gives placement objective as follows:

$$\text{Minimize } WL(\mathbf{x},\mathbf{y}) + \omega \cdot \Delta V_{\max}(\mathbf{x},\mathbf{y}) \tag{19}$$

where ω is the weight of the voltage degradation objective. We compute the voltage degradation weight ω according to the gradients derived from the wirelength and voltage degradation terms so that the scaled voltage degradation gradients are comparable to the wirelength gradients

$$\omega = \beta \cdot \frac{\sum\limits_{x_i,y_j} \left(\left| \frac{\partial WL}{\partial x_i} \right| + \left| \frac{\partial WL}{\partial y_j} \right| \right)}{\sum\limits_{x_i,y_j} \left(\left| \frac{\partial \Delta V_{max}}{\partial x_i} \right| + \left| \frac{\partial \Delta V_{max}}{\partial y_j} \right| \right)} \tag{20}$$

where the voltage degradation ratio β decides the ratio of the voltage degradation gradients to the wirelength gradients and provides a tradeoff knob between voltage degradation and wirelength objectives for the placer.

VI. Experiments

We evaluate our proposed supply voltage degradation aware analytical placement technique by comparing it with an existing supply voltage integrity oblivious analytical placement method APlace [13] on industry designs in a complete VLSI design and analysis flow which is shown in Fig. 3.

We start the physical design flow by specifying power pad locations, creating P/G rings/rails, and performing power routing by Cadence SoC Encounter. The P/G supply networks are extracted by Cadence Fire&Ice. Supply currents for each cell instance in the design are given by Verilog-XL. We then perform supply voltage integrity aware analytical placement, which takes the following as inputs:

1) size and the orientation of each cell instance in the design;
2) supply current of each cell instance;
3) P/G supply network layout;
4) the impedance between any two nodes in the P/G supply networks.

We continue to apply global and detail routing by Cadence TrialRoute and evaluate the resultant P/G supply voltage integrity by Cadence VoltageStorm.

Table I lists some of the key characteristics of the two industry designs that our experiments are based on. Both designs have six metal layers, a P/G ring at the top two layers and four power pads located near the center of the four boundary lines. The AES test case has five power stripes on the second metal layer. The

TABLE I
CHARACTERISTICS OF TEST CASES

Design	# Cells	# Blocks	# Rows	Tech	Utilization
AES	13397	0	129	$90nm$	0.60
PCI	7128	5	251	$180nm$	0.43

TABLE II
CPU RUNTIME (IN SECONDS) AND SUPPLY VOLTAGE DEGRADATION ESTIMATES (NORMALIZED BY SPICE RESULTS) GIVEN BY THE RANDOM WALK SUPPLY VOLTAGE PREDICTION METHOD FOR 8 NODES IN THE POWER SUPPLY NETWORK IN THE AES DESIGN IN 10 AND 100 ITERATIONS, RESPECTIVELY

	#iter \ node	1	2	3	4	5	6	7	8
CPU	10	6.12	8.60	4.74	5.88	4.93	2.12	6.78	7.90
ΔV		0.90	1.13	0.49	0.84	0.48	0.59	1.36	0.96
CPU	100	65.32	71.83	89.02	66.98	92.30	29.04	46.71	74.66
ΔV		1.01	0.99	0.93	0.96	0.94	0.92	0.94	0.96

TABLE III
RESULTS OF MAXIMUM SUPPLY VOLTAGE DEGRADATION AWARE PLACEMENT FOR DIFFERENT SUPPLY VOLTAGE DEGRADATION RATIOS (β's)

Design	Placer	Vdrop Ratio β	Vdrop Analysis				Place		
			Avg Vdrop		Max Vdrop		HPWL		CPU
			(V)	(%)	(V)	(%)	(e8)	(%)	(s)
AES	APlace	0.00	0.233	0.00	0.406	0.00	9.48	0.00	224
	Ours	0.05	0.217	6.61	0.354	12.74	9.58	-1.10	287
		0.10	0.219	6.02	0.356	12.41	9.57	-0.94	266
		0.15	0.214	8.07	0.331	18.49	9.67	-1.95	240
		0.20	0.208	10.67	0.318	21.59	9.68	-2.09	227
		0.25	0.209	10.22	0.314	22.65	9.78	-3.17	218
PCI	APlace	0.00	0.026	0.00	0.051	0.00	19.95	0.00	121
	Ours	0.05	0.025	3.18	0.048	5.54	20.14	-0.93	172
		0.10	0.025	5.84	0.046	9.75	20.25	-1.50	166
		0.15	0.024	9.27	0.044	13.67	20.53	-2.92	156
		0.20	0.023	11.52	0.042	16.65	20.72	-3.87	145
		0.25	0.023	13.08	0.041	19.02	21.01	-5.33	146

PCI test case has four power stripes on the sixth metal layer with five fixed macro blocks.

Table II shows that our proposed stochastic P/G supply voltage prediction method improves estimation accuracy as the iteration number increases, while the runtime and the accuracy of a stochastic P/G supply voltage prediction method vary with the distance between an observation node and a P/G supply pad. For this test case, standard moment computation methods [15] cannot be applied due to their scalability limits; SPICE simulation takes 579.50 s to perform 5000-ps transient analysis in 1 ps time steps; while random walk-based stochastic prediction method provides accurate estimation with less runtime. Random walk-based stochastic P/G supply voltage prediction is especially efficient for system level P/G supply network analysis when a large number of P/G supply pads are present.

Tables III and IV, respectively, give the results of maximum and average supply voltage degradation aware analytical placement. Supply voltage oblivious analytical placement results from APlace are given as reference. For each design, we apply supply voltage degradation aware placement with five different voltage degradation ratios β ranging from 0.05 to 0.25.

The 4th and 6th columns of Tables III and IV show the average and maximum voltage degradation of each placement.

TABLE IV
RESULTS OF AVERAGE SUPPLY VOLTAGE DEGRADATION AWARE PLACEMENT FOR DIFFERENT SUPPLY VOLTAGE DEGRADATION RATIOS (β's)

Design	Placer	Vdrop Ratio β	Vdrop Analysis				Place		
			Avg Vdrop		Max Vdrop		HPWL		CPU
			(V)	(%)	(V)	(%)	(e8)	(%)	(s)
AES	APlace	0.00	0.233	0.00	0.406	0.00	9.48	0.00	224
	Ours	0.05	0.219	6.13	0.361	11.12	9.50	-0.23	284
		0.10	0.210	9.79	0.343	15.48	10.04	-5.88	273
		0.15	0.209	10.19	0.341	16.07	10.12	-6.76	319
		0.20	0.201	13.68	0.320	21.24	10.28	-8.46	312
		0.25	0.192	17.64	0.302	25.70	10.40	-9.74	286
PCI	APlace	0.00	0.026	0.00	0.051	0.00	19.95	0.00	121
	Ours	0.05	0.025	4.94	0.047	6.75	20.22	-1.35	160
		0.10	0.024	9.14	0.044	13.06	21.04	-5.44	175
		0.15	0.019	26.03	0.035	29.80	22.83	-14.45	206
		0.20	0.018	31.02	0.033	35.14	23.18	-16.18	234
		0.25	0.016	39.54	0.028	43.99	25.16	-26.10	285

We also show the improvements in percentage in the 5th and 7th columns. In both tables, the average and maximum voltage degradation results of our placer decreases with the increasing voltage degradation ratio. Either voltage degradation placement objective benefits both metrics at the same time, but with different emphases.

The impact of supply voltage degradation aware placement in terms of HPWL and runtime of the placer are shown in the 8th to 10th columns of Tables III and IV. Supply voltage degradation aware placement usually has a negative impact on these metrics. Placed HPWL increases with the increasing voltage degradation ratio.

We observe that reducing maximum supply voltage degradation leads to better voltage degradation improvements than reducing average voltage degradation, with roughly the same wirelength increase. For example, for the AES test case, reducing maximum supply voltage degradation achieves a 10.2% improvement on the average voltage degradation with 3.2% wirelength increase, while reducing average voltage degradation achieves roughly the same average voltage degradation improvement (10.2%) with larger wirelength increase (6.8%). The same is observed for the PCI test case. A possible explanation is that reducing maximum case supply voltage degradation assigns different weighting factors to the P/G network nodes (in smoothly approximating the max function), which results in more efficient supply voltage degradation reduction for the same amount of wirelength increase.

The voltage degradation ratio (β) can be used as a knob to tradeoff voltage degradation and wirelength. As shown in Tables III and IV, the voltage degradations generally decrease with the voltage degradation ratio increasing; wirelength generally increases with the voltage degradation ratio. A proper value can be chosen according to the practical requirement.

In summary, compared to the reference run by APlace, our supply voltage degradation aware placement reduces maximum supply voltage degradation by 22.7% (19.0%) and average voltage degradation by 10.2% (13.1%), with only 3.2% (5.3%) increase of HPWL for the AES (PCI) test case. Such supply voltage degradation reductions lead to more significant performance improvements due to the superlinear relationship between performance and supply voltage.

VII. Conclusion

We propose stochastic P/G supply voltage prediction and optimization via an analytical placement. We present supply voltage degradation at a P/G node in a function of supply currents, which resembles the Elmore delay formula in a tree-structure P/G network, and can be characterized by effective impedance in a general-structure P/G network via interconnect model order reduction techniques. For efficiency improvement, we propose a random walk-based stochastic prediction method and contraction and interpolation techniques to find effective impedance for supply voltage degradation analysis. We demonstrate that a greedy algorithm finds the optimum placement which minimizes the total voltage drop or the voltage drop at a given node, while finding a placement that minimizes maximum voltage drop over P/G nodes is NP-hard. We also integrate supply voltage degradation into an analytical placement objective in a smooth function. Our experimental results show that the proposed stochastic P/G supply network prediction method achieves 10×–100× speedup compared with traditional SPICE simulation and the proposed P/G supply voltage degradation reduction by analytical placement achieves an average 20.9% (11.7%) improvement of maximum (average) voltage degradation with only 4.3% wirelength increase, and imply further performance improvements.

Our ongoing research includes an extension of the proposed methods to *RLC*(K) P/G supply networks, where ac supply currents and transient or frequency analysis methods are needed, and taking into account the effect of P/G supply voltage degradation in a timing-driven placement framework.

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