Wafer Topography-Aware Optical Proximity Correction

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***Abstract*—Depth of focus is the major contributor to lithographic process margin. One of the major causes of focus variation is imperfect planarization of fabrication layers. Presently, optical proximity correction (OPC) methods are oblivious to the predictable nature of focus variation arising from wafer topography. As a result, designers suffer from manufacturing yield loss as well as loss of design quality through unnecessary guardbanding. In this paper, the authors propose a novel flow and method to drive OPC with a topography map of the layout that is generated by chemical–mechanical polishing simulation. The wafer topography variations result in local defocus, which the authors explicitly model in the OPC insertion and verification flows. In addition, a novel topography-aware optical rule check to validate the quality of result of OPC for a given topography is presented. The experimental validation in this paper uses simulation-based experiments with 90-nm foundry libraries and industry-strength OPC and scattering bar recipes. It is found that the proposed topography-aware OPC (TOPC) can yield up to 67% reduction in edge placement errors. TOPC achieves up to 72% reduction in worst case printability with little increase in data volume and OPC runtime. The electrical impact of the proposed TOPC method is investigated. The results show that TOPC can significantly reduce timing uncertainty in addition to process variation.**

***Index Terms*—Chemical–mechanical polishing (CMP), defocus, dummy fill, optical proximity correction (OPC), topography.**

I. Introduction

As OPTICAL lithography advances into the 90-nm technology node and beyond, minimum feature size outpaces the introduction of advanced lithography hardware solutions. In particular, the minimum depth-of-focus (DOF) margin required for manufacturability of metal layers is extremely difficult to achieve due to nonplanar wafer topography. A root problem is that predictable and systematic variation in DOF is not modeled or exploited during the application of advanced resolution enhancement techniques (RETs) such as optical proximity correction (OPC) and subresolution assist feature (SRAF) insertion. From the designer standpoint, this results in unnecessary guardbanding, difficult performance closure, and wasted (area, delay, and power) chip resources. To the extent that DOF is a determinant of "process window," several works in the literature dealing with process window-aware OPC are worth noting. A work of Cobb and Granik [1] proposes to solve for OPC at a nonzero defocus value to increase DOF, which is the amount of focus variation that can be tolerated while maintaining acceptable lithographic quality. The approach of [1] minimizes an objective that is a function of edge placement error (EPE) and image slope with respect to dose; EPE is the primary objective, and image slope is the secondary objective. The LithoCruiser OPC software from ASML MaskTools [2] can optimize OPC solutions with critical dimension (CD) uniformity median, and yield as objectives. The approach entails Monte Carlo simulation of focus and exposure with Gaussian distributions, as well as aerial image modeling to predict CD. Unfortunately, these and other previous methods are oblivious to "systematic and predictable" focus variation that arises from layout-dependent wafer topography variation. Because deeply subwavelength high-numerical-aperture (NA) lithography is very sensitive to defocus, wafer flatness has become a critical objective for fabrication processes. Chemical–mechanical polishing (CMP) is an enabling technique to achieve thickness uniformity of dielectric and conductor layers in the chip. Dummy fill insertion is a well-known technique to enhance the uniformity of layout feature density to improve the planarization achieved by CMP.[1] Even after dummy fill insertion, there is a great deal of remaining post-CMP topographic variation, which is manifested as dielectric erosion and metal dishing. Post-CMP thickness variations are known to have a severe impact on the stability of downstream process steps and, ultimately, on yield [4]. Defocus corresponding to this thickness variation severely affects patterning of the subsequent upper layer.[2]

OPC is a widely used RET for control of CD. With OPC, photomask shapes are deliberately distorted to compensate for differing amounts of pattern information diffracted at various

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[1]Dummy fill insertion changes the coupling and total capacitance of interconnects [3] and, thus, itself induces design closure issues. However, in this paper, we do not address the question of improved fill synthesis to reduce topographic variation.

[2]There is dielectric deposition and resist spin-on after CMP, and the profile following these two steps is a more accurate representation of the wafer's defocus map. In this paper, we assume that the deposition and spin-on processes conform to the post-CMP profile, as is typically the case.

pitches. Beyond the 130-nm node, SRAF-based OPC with off-axis illumination achieves improved DOF margin. However, tightly prescribed spacing—in particular, assist-to-main pattern and assist-to-assist—are needed to prevent SRAFs from printing [5]. Such layout design constraints result in forbidden pitches with significantly lower printability in certain DOF values [6]. Thus, the industry faces ever-deeper interactions between planarization, defocus, and correct deployment of OPC. This paper is motivated by the fact that current OPC techniques do not consider topography and that this incurs a very large process variability cost. We describe a novel methodology for topography-aware OPC (TOPC) to directly control the CD error that is induced by a nonplanar topography. Different defocus values in a chip are predicted by thickness values that are extracted by CMP simulation. Then, all metal lines with different defocus values are corrected by OPC with different optical/resist models. As a result of the TOPC methodology, we observe significant reduction in CD error, as evaluated by industry-strength OPC and verification flows at the 90-nm node. In this paper, we first present various analyses of lithographic printability for nonplanar topography. We then propose a general methodology for TOPC. Our main contributions are as follows.

- We introduce a novel OPC technique that is aware of post-CMP wafer topography variation. This technique achieves substantial improvement in DOF margin and CD control.
- The TOPC method may lead to poor correction of patterns that are located on the boundary of different DOF values because one pattern is affected by the other (at an incorrect assumed defocus) during the OPC insertion. We assign DOF values to layout features using a reduction to maximum flow to prevent closely spaced patterns from being assigned different defocus values while yet maintaining fidelity to the topography map.
- We investigate the electrical impact of our proposed TOPC method. The results show that TOPC can significantly reduce timing uncertainty and process variation.

The remainder of this paper is organized as follows. In Section II, we present the detailed motivations for our TOPC work. In Section III, we describe our TOPC methodology. Furthermore, we validate TOPC and describe its limitations. In addition, we investigate the electrical impact of our proposed TOPC method. Section IV discusses the experiments and results. Finally, in Section V, we present the main conclusions and ongoing work.

II. Detailed Motivations for TOPC

We motivate our work on TOPC with Fig. 1(a), which shows how post-CMP thickness in copper-oxide polishing will "predictably" change with the region pattern density. The DOF variation corresponding to the thickness variation severely affects metal patterning of the subsequent upper layer, as shown in Fig. 1(b) (results obtained using SOLID-C lithography simulation from Sigma-C). In this figure, t_1 and t_2 are post-CMP thickness variations over dense and sparse regions, respectively. In this paper, we investigate the impact of focus variation on CD in nontransitional regions. However, we show (in Section IV) that TOPC can be applied to transitional regions without degradation in its quality.

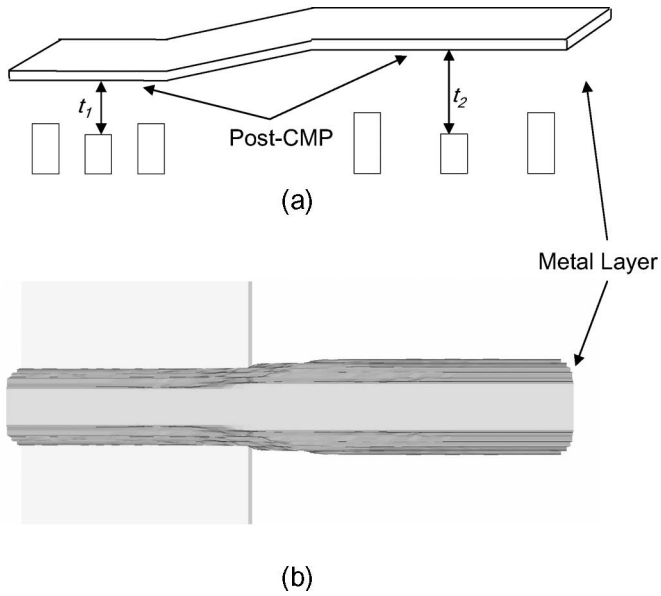

Fig. 1. (a) Side view showing thickness variation over regions with dense and sparse layout. (b) Top view showing CD variation when a line is patterned over a region with uneven wafer topography, i.e., under conditions of varying defocus.

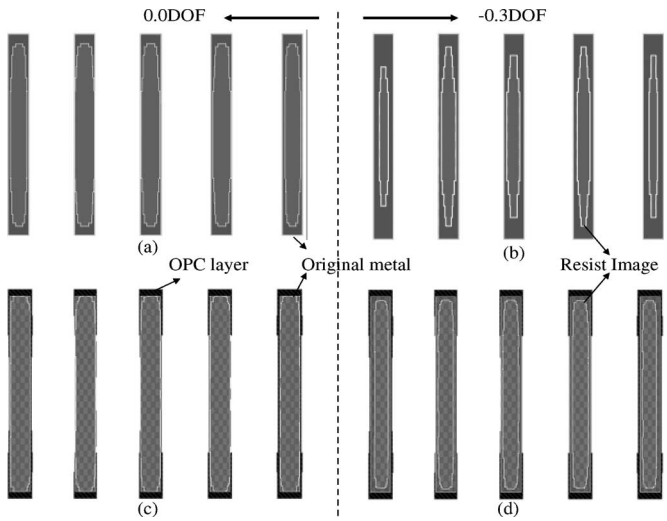

Fig. 2. Standard OPC simulation. (a) Original layout (drawn shape) and simulation result with zero DOF model. (b) Original layout and simulation result with -0.3-μm DOF model in the nonplanar topography. (c) Standard OPC layout and simulation result with zero defocus model. (d) Standard OPC layout and simulation result with -0.3-μm DOF model in the nonplanar topography.

A. Standard Versus TOPC and Optical Rule Check (ORC)

We also motivate wafer TOPC by considering the gap between focus awareness and focus unawareness not only in the OPC insertion but also in the ORC step that checks post-OPC printed images against drawn shapes. We distinguish two kinds of OPC methodology, namely: 1) standard and 2) topography-aware. In standard OPC (SOPC), the assumption is that any particular layer is flat, and therefore, a defocus value of zero is considered for that layer. This incorrect assumption will lead

TABLE I
FOUR DIFFERENT COMBINATIONS OF OPC AND ORC: STD AND T-A INDICATE STANDARD AND TOPOGRAPHY-AWARE METHODOLOGIES, RESPECTIVELY

OPC method	ORC method	Δ CD (Drawn vs. Printed)
STD	STD	~ 0
STD	T-A	> 0
T-A	STD	> 0
T-A	T-A	~ 0

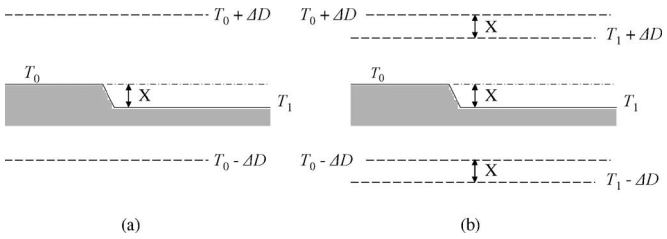

Fig. 3. (a) Example of (SOPC + SORC) and (SOPC + TORC). (b) Example of (TOPC + SORC) and (TOPC + TORC). X is the thickness variation.

to CD variation of the metal feature that will be placed on that layer. To clearly illustrate the CD variation in SOPC, Fig. 2 compares the resist image of metal lines in 0.0-μm DOF with the image in -0.3-μm DOF. CDs of metal lines in -0.3-μm topography are not correct after SOPC with zero defocus, although CD degradation after the OPC is somewhat better than before OPC. On the other hand, if the thickness variation of the layer is taken into account, OPC can adjust its process accordingly. Considering OPC and ORC together, there are four combinations, as shown in Table I. We explore the effectiveness of each combination separately in the following discussion.

In Table I, STD and T-A stand for standard and topography-aware methodologies, respectively. To explain these combinations, assume that in 90-nm technology, the maximum allowable defocus value is ± 0.3 μm (ΔD) for manufacturing. We also refer to the thickness variation of the layer as X. We wish to make the case that when both OPC and ORC are topography aware, CD variation will be minimized.

- Fig. 3(a) shows the case when the combination of standard OPC and standard ORC is used. Standard OPC ignores thickness variation; hence, pattern on T_1 layer is assigned the same defocus as T_0 layer. If there is no thickness variation, this combination leads to a small CD variation because OPC can easily exploit the pitch dependence of CD. However, the problem with this method is that the premise of an even topography is wrong. In other words, due to CMP process effects, the layer is not exactly flat.
- Fig. 3(a) also shows the case when SOPC is used with topography-aware ORC (TORC). In this case, there is still no consideration of thickness variation during the OPC process, but ORC is aware of the topography, which changes the maximum allowable defocus value set by ORC. In general, the maximum allowable defocus value set by TORC is derived as $T_i \pm \Delta D$, where T_i is the defocus value set for each specific region of the layer and ΔD is the maximum allowable defocus value set by standard ORC. Since SOPC assigns zero defocus to the layer, the maximum allowable range for ORC is only $\pm \Delta D$. On the other hand, TORC has been adjusted according to the topography. In this paper, zero, plus, and minus defocus represent the nominal thickness (height), greater than nominal, and less than nominal thickness, respectively. In Fig. 3(b), we assume that T_0 has zero defocus and T_1 has -0.1-μm defocus. This changes the maximum allowable defocus value set by ORC; for T_0, we have a range of -0.3 to 0.3, and for T_1, the range is from -0.4 to 0.2. Since the allowable range for SOPC is from -0.3 to 0.3, there is a mismatch between OPC and ORC. This generates an ORC error on T_1 layer.
- The third combination, which employs TOPC and standard ORC, is not of interest. As with the first combination, the entire premise of the scenario is faulty: OPC is aware of the topography and adjusts accordingly, but standard ORC does not consider the changes. For example, T_1 that has a defocus value of -0.1 will have an allowable defocus range of -0.4 to 0.2, but standard ORC still considers a range of -0.3 to 0.3 as shown in Fig. 3(b). This again generates an ORC error on T_1 layer similar to second combination.
- The final combination should yield the best result because both the OPC and ORC are aware of the topography and therefore can adjust accordingly as shown in Fig. 3(b). For example, T_0 will have an allowable defocus range of -0.3 to 0.3, whereas T_1 will have a defocus range of -0.4 to 0.2. Thus, the pattern on T_1 will meet CD tolerance with -0.4-μm DOF.

B. Cost and Quality of OPC

Increased application of OPC makes mask data preparation difficult: figure counts explode as dimensions shrink and RETs are more heavily used [7]. To optimize the data volume, conventional OPC hierarchically reorganizes the input graphic data system (GDSII) data by reducing the redundant representation of identical cells [8]. The spatial context consisting of such identical cells is a monolithic "unit" as the proximity correction process evaluates effects due to adjacent or nearby features within the optical radius of influence. Thus, identical contexts are corrected only once, which helps reduce correction time and data volume. Our proposed TOPC methodology affects hierarchical decomposition of the layout because "context" must now be with respect to both the proximity effect of neighboring patterns and the DOF values of the topography. In particular, identical patterns that are assigned to different DOF values are no longer together within the same context, and all context information should be newly constructed according to patterns that have the same DOF value. In the TOPC methodology, all figures are partitioned among a relatively small number of DOF values. The number of DOF values used in this partitioning (see Section III-A) must be carefully considered, as increasing this number negatively impacts data volume and OPC runtime, even as TOPC achieves better CD control and DOF margin.

III. TOPC METHODOLOGY

To account for defocus change induced by a nonplanar topography, we add CMP simulation and layer generation for DOF making into the standard design flow. Fig. 4 shows the

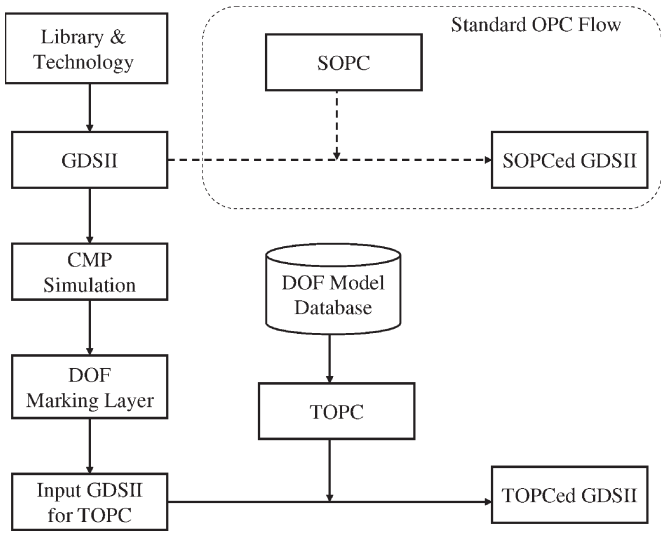

Fig. 4. Comparison of design flow with standard OPC and TOPC methods. A map of thickness variation from CMP simulation is converted to DMLs and then fed into GDSII for TOPC.

comparison of design flow with standard OPC and TOPC methods. SOPC uses a standard GDSII layer as an input and then correct pattern proximity under zero defocus assumption. A novel TOPC method first uses a CMP simulator[3] to compute a topographic map over the chip layout. The derived CMP simulator uses a predictive mathematical model of pattern dependencies in Cu CMP processes, which consists of three steps. In the first step, the time to remove the overburden Cu is calculated. The second step deals with the removal of the barrier material. During this step, due to clearing of the barrier, Cu dishing occurs. In addition, due to nonuniform pattern density within a die, different locations in the die will be cleared at the different times, which cause overpolishing certain features. Finally, in the third step, the amount of Cu dishing and oxide erosion is calculated [18]. Using dishing and erosion parameters, the simulator will associate a height to every feature in the layout. We then pass the associated heights into our DOF marking layer (DML) generator as input. DML generator assigns an associated DOF value for each feature, and its DOF values are represented by GDS layer. Thus, new input GDSII for TOPC is consisted of original standard layout and DOF marking layer. Given total DOF variations, precharacterized DOF models database can be used for TOPC pattern optimization. Our new OPC recipe invokes a particular DOF model corresponding to assigned DML for each feature during TOPC. Thus, TOPC can compensate for CD distortions induced by pattern proximity and DOF errors.

A. DML Assignment

While the CMP simulation yields a continuous topographic map, it is necessary and practical to use only a small number of discrete defocus values when calculating the OPC solution. Thus, the central problem is to assign one of the available defocus values to each layout feature while reflecting the topographic map as accurately as possible. In our methodology, every layout feature f_i is associated with DML(f_i), which indicates the defocus value (e.g., $+0.1$ μm) that is assumed during the calculation of resolution enhancement (e.g., OPC or phase-shifter mask) for f_i. However, applying two different OPC models to two adjacent patterns on some boundary will increase CD variation compared to using an "average" DOF model. For example, to correct one pattern on the 0.1-μm DML boundary, the pattern should refer to the image of other patterns on the 0.2-μm DML boundary. However, these other patterns are being simulated by a 0.1-μm DOF model instead of a 0.2-μm DOF model. In this case, CDs of the two patterns can be more distorted than if, e.g., we apply to all patterns a 0.15-μm DOF model that is the average of the two models. Accuracy of resolution enhancement (as well as inherent limitations of OPC software) requires that $\text{DML}(f_i) = \text{DML}(f_j)$ for all features f_i, f_j whose interfeature distance $d(f_i, f_j) \leq R$, where R is the "optical radius" of the lithography process. This requirement grows stronger as the interfeature distance $d(f_i, f_j)$ decreases. In modern lithography processes, typical values of R are on the order of 1 μm or less. The interfeature distance requirement of the DML assignment can be captured using a graph in which each feature is represented by a vertex, and there is an edge between two vertices if the distance between their corresponding features is less than R. We may further assign weights to edges in this graph, with higher edge weights corresponding to pairs of features that are closer to each other. The other requirement is that every feature should be assigned to the DML partition to which it normally belongs, if possible.

We formalize the problem of assigning features to k DMLs as follows: Given a set of vertices $V = \{v_1, v_2, \ldots, v_n\}$ with height function $h : V \rightarrow Z^+$,[4] where Z^+ is the set of natural numbers, a set of weighted edges $E \subseteq V \times V$, and $2k-2$ threshold values $\text{Th}_1, \text{Th}_2, \ldots, \text{Th}_{2k-2}$. The minimum value of $h(v)$ is Th_0, and the maximum value of $h(v)$ is Th_{2k-1}. Our methodology for assignment of features to k DMLs is detailed in Fig. 5. Lines 1 and 2 set up a topographic map with our CMP simulation model. We perform $k-1$ minimum cut bipartition to determine the DML assignments in lines 3–7. During each iteration, we want to find the features that are assigned to DML l $(1 \leq l \leq k-1)$ and remove them from the future flow networks. Line 4 constructs a flow network topology for the bipartition. Two supernodes S and T in the network are to be assigned to different partitions. All features in the same partition as S in the bipartition solution will be assigned to DML l. In line 5, we add an infinite-capacity edge from S to v_i for all features f_i with $h(f_i) \leq \text{Th}_{2l-1}$. Therefore, we can guarantee that these features are assigned to DML l in the final bipartition solution. Similarly, an infinite-capacity edge from T to v_i for all features f_i with $h(f_i) \geq \text{Th}_{2l}$ is added to ensure that these features are not assigned to DML l. The other features with $\text{Th}_{2l-1} < h(f_i) < \text{Th}_{2l}$ can be assigned to either partition with two soft constraints: 1) two features within the optical radius should be put in the same partition, if possible and 2) each

[3]Commercial CMP simulation software is available from companies such as Praesagus [9]. In our current implementation, we use a CMP simulation model derived from the Ph.D. thesis of Tugbawa [10].

[4]$h(f_i)$ is the thickness value of the CMP simulation tile, in which the geometry center of the feature f_i is located. The size of tile is primarily determined by the interaction length in CMP process (100–200 μm for Cu CMP). In this paper, a tile size of 10 μm is chosen.

Input: Layout data in GDSII Stream format, optical radius R,
defocus marking layer thresholds $Th_1 < Th_2 < ... < Th_{2k-2}$

Output: Partition of all features into k DMLs

1. Use CMP simulation to compute the post-CMP topography
2. From the topography, determine the height $h(f_i)$ for each feature f_i
3. **For** $(l = 1; l \leq k-1; l{+}{+})$
4. Construct a flow network topology $N = (V,E)$ with a vertex v_i for each feature f_i, a super-source S and a super-sink T, and an edge $e_{i,j}$ between two vertices v_i and v_j if $dist(f_i, f_j) < R$
5. Calculate edge capacities in the flow network N as follows
   (A) If $h(f_i) \leq Th_{2l-1}$, there is an infinite-capacity edge from S to v_i.
   (B) If $h(f_i) \geq Th_{2l}$ then there is an infinite-capacity edge from v_i to T
   (C) If $Th_{2l-1} < h(f_i) < (Th_{2l} + Th_{2l-1})/2$, then there is an edge from S to v_i with weight $(Th_{2l} + Th_{2l-1})/2 - h(f_i)$
   (D) If $(Th_{2l} + Th_{2l-1})/2 \leq h(f_i) < Th_{2l}$, then there is an edge from v_i to T with weight $h(f_i) - (Th_{2l} + Th_{2l-1})/2$
   (E) For all edges $\in N$, edge capacities are given by the weights $w(e_{i,j}) = \lfloor \frac{R}{dist(f_i,f_j)} \rfloor$
6. Calculate a maximum S-T flow in the edge-capacitated flow network N.
   The maximum flow saturates a min-weight cut
7. All vertices on the S side of the cut are assigned to DML l and deleted
8. The remaining vertices are assigned to DML k

Fig. 5. k DML assignment methodology.

feature should be assigned to the partition to which it normally belongs to reduce the thickness variation within each DML partition, if possible. To quantify these two conflicting requirements and achieve the best tradeoff between them, we add an edge $e_{i,j}$ of the weight $\lfloor R/\text{dist}(f_i, f_j) \rfloor$ between two vertices v_i and v_j if $\text{dist}(f_i, f_j) < R$ for the first requirement. Similarly, we add an edge from S to v_i for all the features with $\text{Th}_{2l-1} < h(f_i) < (\text{Th}_{2l} + \text{Th}_{2l-1})/2$ and an edge from v_i to T for all the features with $(\text{Th}_{2l} + \text{Th}_{2l-1})/2 \leq h(f_i) < \text{Th}_{2l}$ for the second requirement. Therefore, a "cut" in the network represents the violation of one of the two soft requirements. The minimum cut bipartization solution has the minimum violation for the two requirements. In lines 6 and 7, we solve the minimum cut bipartition problem and assign the features on the S side to DML l.

B. TOPC Validation and Limitations

Our previous work [11] proposed one form of TOPC validation methodology. However, that DML-based TORC may not be accurate enough since we use only a few DML to reduce the OPC complexity. In this paper, we present an enhanced TORC methodology that is based on thickness value for each CMP simulation tile [12]. As a result, the number of TORC models is increased, and CD printability can be evaluated using more DOF values. We also discuss practical limits of TOPC as deployed using current commercial software tools.

Suppose the given CD tolerance for manufacturing of all patterns, generally $\pm 10\%$ of each pattern size, is satisfied with given worst case defocus. Then, we can assume that the maximum allowable defocus range ΔD is comprised of topography variation (50% contribution) and other factors (50% contribution). Thus, topography variation contributes half of the worst case DOF value. We compare QOR of TOPC and standard OPC as follows.

- DMLs are generated based on thickness value and k DML algorithm.
- Different DOF OPC models are applied to the DMLs to compensate for CD error induced by topography.

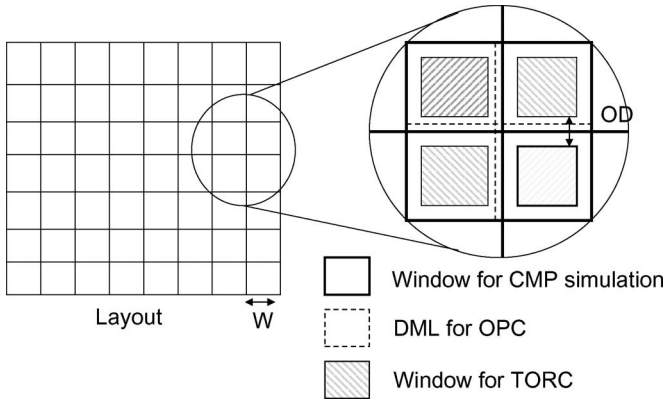

Fig. 6. TOPC validation regions.

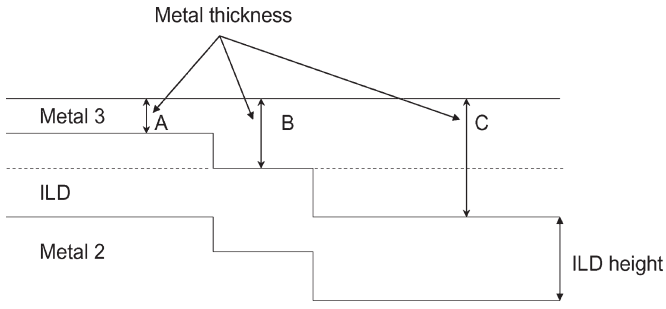

Fig. 7. Thickness variation after metal deposition.

- For each feature, we calculate different worst case defocus values according to the thickness (height) value of its window in the CMP simulation. One DML may include several CMP simulation tiles within a range of thickness values. Thus, our new methodology increases the number of TORC models.
- We compare the numbers of CD violations that occur with standard OPC versus TOPC.

To validate the TOPC methodology, we only consider two combinations, namely 1) STD OPC/T-A ORC and 2) T-A OPC/T-A ORC. The other two combinations are ignored since

TABLE II
COMPARISON OF THE TIMING DELAY USING SOPC AND TOPC; THE UNITS FOR WIDTH, t_{metal}, h_{ILD}, C/μm, R/μm, AND DELAY ARE NANOMETERS, NANOMETERS, NANOMETERS, FEMTOFARADS, OHMS, AND PICOSECONDS, RESPECTIVELY

TOPC							
Case	width	t_{metal}	h_{ILD}	$C/\mu m$	$R/\mu m$	delay	
1	140	250	350	0.142	0.629	2.429	
nominal	140	350	350	0.174	0.449	2.415	
2	140	450	350	0.211	0.349	2.427	
SOPC							
Case	width	t_{metal}	h_{ILD}	$C/\mu m$	$R/\mu m$	delay	%diff
nominal	140	350	350	0.174	0.449	2.415	0
3	162	250	350	0.165	0.543	2.752	-11.8
4	118	250	350	0.126	0.746	2.206	9.2
5	162	450	350	0.248	0.302	2.770	-12.4
6	118	450	350	0.183	0.414	2.187	9.9

(as discussed in Section II-A) they are based on incorrect premises. Since current commercially available OPC software tools do not accurately consider the transient region of topography, we only apply the TORC to features that do not lie on the boundary between two different defocus values. The TOPC is applied to all regions, including the regions to which TORC cannot be applied due to commercial OPC tool limitations. In Fig. 6, TORC will be applied to the hatched areas while TOPC will be used in all areas. The distance between the regions to which TOPC will be applied is equal to the optical diameter. Despite this constraint, we show in the next section that TOPC substantially reduces CD error in regions where it can be applied. In addition, we investigate how TOPC impacts the CD error in the transient region of topography.

C. TOPC Electrical Impact

To validate the electrical impact of the TOPC methodology, i.e., in achieving more accurate performance analysis, we use a testbed consisting of three parallel 5000-μm semiglobal lines in 90-nm technology. After CMP planarization, we assume that there are three different defocus values and correspondingly three metal thickness values. Fig. 7 shows metal lines with thickness values A, B, and C located at plus defocus, nominal defocus, and minus defocus, respectively. Interlayer dielectric (ILD) is located between metal 2 and metal 3 layers. In this experiment, assuming a $\pm$100-nm ILD height variation, we have run simulations for nominal height ($= 0.35\ \mu$m) as well as heights due to plus and minus defocus topography, 0.25 μm and 0.45 μm, respectively. Topography and defocus seen by metal 3 layer comes from ILD height variation, which, in turn, is a result of both post-CMP variation on metal 2 and conformal ILD deposition. Hence, metal 3 thickness is inversely proportional to metal 2 thickness. This assumes perfect CMP on metal 3. Table II has captured different possible scenarios and their corresponding results.

Mentor Graphics Calibre WORKbench v9.3_5.9 is used to measure the CD and line spacing [17]. In SOPC, there are wire segments with larger EPE after TORC is applied to GDS. For those segments, we measure the CD difference after TORC with TOPC GDS. In this experiment, we used $\pm$100-nm thickness variation with the maximum CD difference of $\pm$22 nm. The nominal width and spacing of each conductor are 0.14 and 0.14 μm, respectively. The nominal per-micron capacitance and resistance of each conductor, as estimated by Berkeley Predictive Technology Model interconnect models [13], are 0.174 fF and 0.449 Ω, respectively. To reflect actual design context, we buffer each interconnect according to closed-form equations from [14].[5]

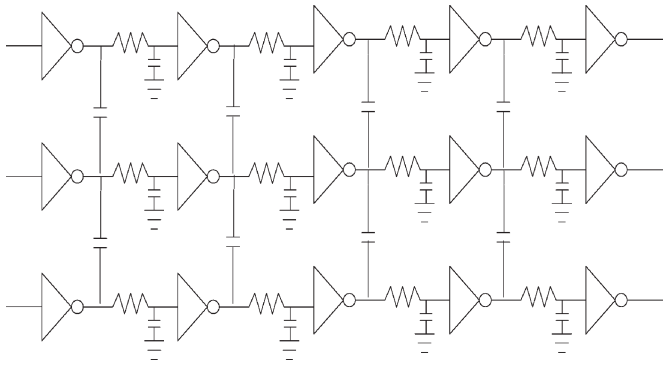

Fig. 8. Schematic of a buffered interconnect system.

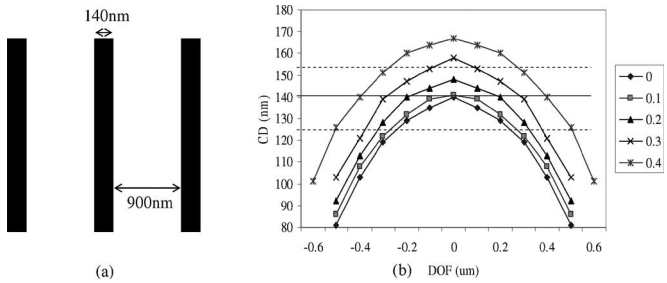

Fig. 9. (a) Line-and-space test pattern with 0.14-μm linewidth and 0.9-μm space. (b) Comparison of DOF and CD improvements with SOPC and TOPC. The five curves from 0 to 0.4 represent OPC patterns with models of 0–0.4 DOF values.

Fig. 8 shows a system of three parallel buffered interconnect that is used in our experiment. Using the above parameters, we configure our buffered interconnect system in Synopsys HSPICE U-2003.09 to compute circuit delay [19]. As described above, CD difference between SOPC and TOPC is $\pm$22 nm for $\pm$100-nm ILD height variation. Assuming an ILD height

[5]The buffers are inserted at equal distances along each interconnect, i.e., at positions 1000, 2000, 3000, and 4000 μm from the driver.

TABLE III
COMPARISON OF DOF MARGIN WITH TOPC AND SOPC: TOTAL DOF MARGIN OF TOPC INCREASES BY 0.14 μm COMPARED TO SOPC

OPC method	Topography thickness (μm)	- directional DOF margin (μm)	+ directional DOF margin (μm)	Total DOF margin (μm)
SOPC	0.0	0.25	0.25	0.50
SOPC	0.1	0.35	0.15	0.50
SOPC	0.2	0.45	0.05	0.50
SOPC	0.3	0.48	0.00	0.48
TOPC	0.0	0.25	0.25	0.50
TOPC	0.1	0.38	0.18	0.56
TOPC	0.2	0.52	0.12	0.64
TOPC	0.3	0.49	0.09	0.58

variation of ± 100 μm and three different metal thickness values, we have considered seven possible cases. According to the results in Table II, SOPC can result in timing error up to 12.4%.

IV. EXPERIMENTS AND RESULTS

We use two benchmark designs in our experiments. The first benchmark (Benchmark1) is the alu128 core with 8.7K instances from Artisan libraries in a 90-nm technology using Synopsys Design Compiler v2003.06-SP1. The synthesized netlists are placed with row utilization of 90% using Cadence First Encounter v3.3. The second benchmark (Benchmark2) consists of combined aes and des cores with 189K total placable instances and 65% row utilization, also from Artisan libraries in a 90-nm technology. The netlists of both designs have been obtained from "OpenCores" [15]. All designs are trial routed before running timing analysis. On the lithography side, we use Sigma-C SOLID-C v3.0 to investigate CD impact of topography. CalibreOPC, CalibreOPCsbar, and CalibreORC from Mentor Graphics Calibre v9.3 5.11 are used for model-based OPC, SRAF generation, and ORC, respectively.

First, we evaluate how TOPC impacts DOF enhancement and CD control using a simple test structure. Fig. 9(a) shows the simulation results of three-bar line-and-space patterns with 140-nm linewidth and 900-nm space. The five curves from 0 to 0.4 represent OPC patterns with models of 0–0.4 DOF values. CDs of the five different OPC patterns on X-axis from lithography simulation results using 0.0- to 0.6-μm DOF model are plotted. SOPC corrects CD error with only a zero DOF model, i.e., SOPC compensates for only pattern proximity error under zero DOF. For example, if the pattern corrected by SOPC is located at 0.3-μm topography, CD of the pattern is 119 nm as shown Fig. 9(b) (see a curve representing OPC patterns applied to zero OPC model). Thus, the pattern violates CD tolerance, which is typically $\pm 10\%$ of 140-nm nominal pattern size. On the other hand, if we apply TOPC with 0.3-μm DOF model to the pattern on 0.3-μm topography, CD of the pattern is 127 nm, which is within our tolerance (see a curve representing OPC patterns applied to 0.3-μm OPC model.). Thus, we obtain better printability with TOPC.

Table III summarizes the experimental results. The total DOF margin of OPC pattern on a particular topography is the sum of $+$ and $-$ directional DOF margins. DOF margin of SOPC corresponds to the margin of the curve with 0 DOF, while DOF margins of TOPC are different for 0 to 0.4 OPC models. For example, if a pattern is located at 0.2-μm topography, $+$ directional DOF margins of SOPC and TOPC are 0.05- and 0.12-μm DOFs, respectively. $-$ directional DOF margin of SOPC is 0.45 μm, while TOPC is 0.52 μm. Thus, the total DOF margin of TOPC increases by 0.14 μm compared to that of SOPC.

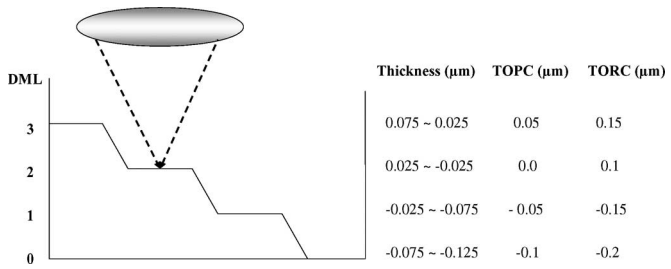

Fig. 10. Example of topography with 0.2-μm thickness variation. Y-axis represents thickness error, DOF model used in TOPC, and DOF model used in TORC.

Second, we compare the CD impacts in transient region with TOPC and SOPC. As shown in Section III-B, the TORC is not applied to all regions due to tool limitation. Thus, we assume that the pattern located at the transient region has average DOF values of the two adjacent DMLs. Three-bar line-and-space patterns (140-nm line and 900-nm space) are used again to check the CD quality in the transient regions. Fig. 10 shows an example of topography for a testcase with 0.2-μm thickness variation. We assume that the stepper machine focuses on DML2. Table IV shows the CD errors of TOPC and SOPC in the given topography. DOF models for TOPC in the transient region are assigned by smaller one of adjacent two DOF values. QORs of patterns in the region are evaluated using average DOF model. The results of TOPC regions are much better than that of SOPC even for patterns in the transient regions.

Finally, we implemented the k DML assignment methodology in C++ as shown in Fig. 5. As the number of DML k increases, the number of contexts that the OPC engine has to handle also increases [16]. This leads to flattening and hence an increase in the OPC runtime. For each DML, qualified optical and process models are also needed. Each additional DML will introduce significant overhead in terms of test, measurement, and process model calibration. Thus, our choice of $k = 4$ for the number of DMLs is carefully made: This is the smallest number of DMLs that will satisfy the fact that the stepper machine does not always focus on the center of the topography.

Our DML assignment algorithm is used for two industry benchmark designs. The Benchmark1 testcase has 6127 features, and the Benchmark2 testcase has 933 985 features. The optical radius R is set as 0.64 μm. The runtimes of k DML assignment for Benchmark1 and Benchmark2 are 0.31 s and 38.7 s, respectively. All tests are run on a hyper-threaded Intel

TABLE IV
COMPARISON OF CD QUALITY WITH TOPC AND SOPC IN TRANSIENT REGIONS: CD ERROR IN TOPC CAN BE REDUCED BY UP TO 13 nm

DML	Model for TOPC (μm)	Model for SOPC (μm)	Model for QOR (μm)	CD error with TOPC (nm)	CD error with with SOPC (nm)
3	0.05	0.0	0.05	1	6
$2 \sim 3$	0.0	0.0	0.025	3	3
2	0.0	0.0	0.0	1	1
$1 \sim 2$	-0.05	0.0	-0.025	4	3
1	-0.05	0.0	-0.05	1	7
$1 \sim 0$	-0.1	0.0	-0.075	4	10
0	-0.1	0.0	-0.1	1	14

TABLE V
COMPARISON OF EPE COUNT REDUCTIONS WITH SOPC AND TOPC

Testcase	Thickness variation (nm)	Reduction of EPE Count with +/- 6nm EPE range (%)	Reduction of EPE Count with +/- 7nm EPE range (%)
Benchmark1	+/- 30	9.2	10.7
	+/- 60	22.3	29.1
	+/- 100	34.9	52.3
Benchmark2	+/- 30	14.3	15.2
	+/- 60	38.1	39.4
	+/- 100	48.1	67.0

TABLE VI
COMPARISON OF WORST CASE EPE COUNTS WITH SOPC AND TOPC

Testcase	Thickness variation (nm)	EPE Count for Ranges exceeding +/- 14nm in SOPC	EPE Count for Ranges exceeding +/- 14nm in TOPC	Percentage Improvement (%)
Benchmark1	+/- 30	21	9	57
	+/- 60	35	12	66
	+/- 100	47	16	66
Benchmark2	+/- 30	55	20	64
	+/- 60	99	31	69
	+/- 100	119	34	72

Xeon 2.4-GHz CPU. For each testcase, we assumed three different polish times in the CMP model, which leads to three different thickness variations: 0.06, 0.1, and 0.2 μm. For the case of 0.2-μm maximum thickness variation, we can generate four different DMLs with 0.05-μm step size[6] for metal 3. Specifically, DML 0 represents all metal lines with topography thickness of 0.0–0.05 μm; DML 1 has metal lines with added 0.05-μm step size, i.e., 0.05–0.1 μm, and DML 2 and DML 3 are similarly assigned.

TOPC is applied to each DML with models whose DOF values are based on the average thickness value of the corresponding DML. Assuming that the Bossung plots are symmetrical with respect to 0-μm defocus (e.g., -0.05 and 0.05 μm are considered the same as shown in Fig. 10), metal lines have three different DOF values. TORC is performed with worst case DOF models as in Section III-B. The nontopography factors ΔD account for 0.10-μm defocus in the testcase with 0.2-μm thickness variation. As a result, a pattern with 0.05-μm thickness error will have worst case DOF of 0.15 μm. Fig. 10 shows thickness, DOF model used in TOPC, and DOF model used in TORC. Each OPCed metal line in the hatched areas is evaluated by TORC with different worst case DOF models. We apply this methodology to both the Benchmark1 and Benchmark2 testcases.

TOPC benefits increase for larger EPE range and chip size [11]. Thus, we evaluate how TOPC impacts printability improvement for different chip sizes and EPE ranges. Table V shows the improvement of TOPC with respect to EPE Count, which is the number of edge fragments on metal having CD error greater than or equal to a certain threshold. Each testcase is validated according to two EPE Count criteria, i.e., EPE Count with ± 6 nm (± 7 nm) EPE range that represents the number of edge fragment having CD error from 6 nm (7 nm) to -6 nm (-7 nm). After TOPC, EPE Counts of Benchmark1 and Benchmark2 are reduced by 9.2%–52.3% and 14.3%–67.0%, respectively, under various thickness variation regimes, as shown in Table V. TOPC is increasingly effective in compensating for CD error as the wafer topography exhibits more thickness variation. Moreover, average improvement of Benchmark2 is larger than that of Benchmark1 since larger chip is exposed by more topography variation.

We define worst case EPE Count as the number of edge fragments with EPE exceeding ± 14-nm EPE, which is $\pm 10\%$ of 140-nm nominal metal line in both benchmark designs. The worst case EPE may translate to functional faults such as notching and bridging of patterns. Pattern fragments with the worst case EPE are more sensitive to other variations such as chip-to-chip, wafer-to-wafer, and machine-to-machine. Hence, the worst case EPE has been a typical measure of functional faults in industry practice as we consider more variations. TOPC reduces the number of worst case EPEs by up to 72% as shown in Table VI. The improvements in process window and potential yield come at the cost of some increase in data volume and OPC runtime, as shown in Table VII due to hierarchy flattening and context increase of TOPC. However, the increased costs of data volume and runtime are negligible compared to the large printability improvement.

[6]The step size is calculated as total thickness variation divided by the number of required DMLs.

TABLE VII
COMPARISON OF OPC RUNTIME AND DATA VOLUME BETWEEN SOPC AND TOPC

Testcase	Original GDS (MB)	SOPC GDS (MB)	SOPC Runtime (min.)	TOPC GDS(MB)	TOPC Runtime (min.)
Benchmark1	5.0	7.2	17	9.4	22
Benchmark2	696.2	2706.7	3351.1	3073.4	3459.7

V. CONCLUSION AND ONGOING WORK

In this paper, we have proposed the first methodology for wafer topography-aware OPC. With an experimental testbed of 90-nm foundry libraries, industry OPC recipes, and commercial OPC and ORC software tools, we have confirmed that our technique achieves up to 67% reduction in EPEs at $\pm$100-nm thickness variation. In particular, TOPC can achieve up to 72% worst case printability problem reduction such as notching and bridging of patterns.

Our research on the electrical impact of the proposed method shows that the timing uncertainty is reduced. With dimensions scaling faster than the lithographic process, DOF and hence awareness of topographic variation in RET will become increasingly important. Thus, we believe that topography-aware techniques will be critical for reducing parametric variation—particularly of interconnect performance—in future technology nodes. Our ongoing work is in the following directions.

- Lithographic process window is one of the most important reasons for stringent requirements for the CMP and dummy fill processes. A TOPC flow will enable reduction in layout density control requirements and hence the design impact (e.g., capacitive coupling overhead) of dummy fills. We are investigating the interaction between dummy fill and OPC in this context.
- Assist features are inserted in the OPC flow to increase DOF of isolated features. TOPC uses more accurate "nominal" focus values locally, which can lead to a reduced complexity of assist feature insertion flows. We are currently investigating this synergy.
- We are currently investigating ways in which the DML partitioning flow can be made more design aware. For example, there are several ways in which timing and power constraints can inform the steps of DML construction and feature assignment to DMLs.
- Finally, we are investigating improved TOPC and TORC flows to handle geometries at the edges of a DML (recall that we currently ignore such geometries).

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