Methodology for Electromigration Signoff in the Presence of Adaptive Voltage Scaling

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***Abstract*—Electromigration (EM) is a growing reliability concern in sub-22*nm* technology. Design teams must apply guardbands to meet EM lifetime requirements, at the cost of performance and power. However, EM lifetime analysis cannot ignore front-end reliability mechanisms such as bias temperature instability (BTI). Although the gate delay degradation due to BTI can be compensated by adaptive voltage scaling (AVS), any elevated supply voltage will accelerate EM degradation and reduce lifetime. Since the degradation of BTI is front-loaded, AVS can increase electrical stress on metal wires relatively early during IC lifetime, which can significantly decrease electromigration reliability. In this paper, we study the "chicken-egg" interlock among BTI, AVS and EM and quantify timing and power costs of meeting EM lifetime requirements with full consideration of BTI and AVS mechanisms. By applying existing statistical and physical EM models, we demonstrate that without such considerations, the inaccuracy (reduction) of EM lifetime due to improper guardband against BTI at signoff can be as high as 30% in a 28*nm* FDSOI foundry technology. Furthermore, we provide signoff guidelines which suggest that the lifetime penalty can be compensated by paying a penalty of up to 1.6% in area and 6% in power. We also demonstrate that suboptimal choice of voltage step size and scheduling strategy can result in up to 1.5 years of decreased EM lifetime.**

I. Introduction

Reliability signoff is critical in modern sub-22*nm* technology nodes to guarantee that an IC product operates at a minimum acceptable performance through out its lifetime [14]. Recently, the most important reliability mechanisms for IC design teams are bias temperature instability (BTI) and electromigration (EM) [14] [30] [31]. BTI degrades chip performance by slowing down device switching speeds in critical paths. EM can increase wire resistance, which can cause voltage drop resulting in device slowdown; it can also cause permanent failures in circuits due to shorts or opens. To meet performance requirements, design teams overcome performance degradation due to BTI by applying adaptive voltage scaling (AVS) [8]. To meet lifetime requirements, design teams overcome mean time to failure (MTTF) with respect to EM-induced interconnect voids and shorts by applying design guardbands [19] [13] [24] [21]. Sometimes, design teams can try to make interconnects 'immortal' by limiting segment lengths to be less than or equal to the Blech length [7]. However, recent analysis shows that immortality is not guaranteed under all operating conditions [21]. The authors of [21] demonstrate that under long-time electrical stress, all power and ground interconnects suffer from EM degradation which results in larger wire resistances and can cause supply voltage drop (IR drop). IR drop can result in delay degradation and timing failures.

Even as modern designs use AVS to compensate the delay degradation, the higher supply voltages can accelerate EM failures [14]. Hence, design teams are forced to use larger margins to guardband against delay degradation, that is, sign off at either a lesser lifetime or lesser performance. This dilemma induces a "chicken-and-egg" loop in the signoff flow as shown in Figure 1. To our best understanding, the interaction between BTI-induced AVS and EM in the context of this chicken-and-egg loop has not been studied in previous works. This motivates us to study EM-aware signoff for systems that use AVS.

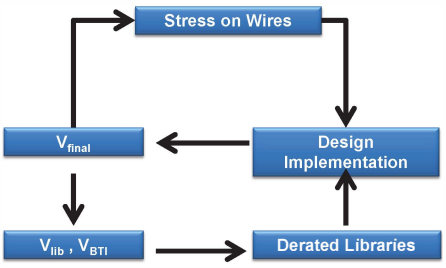


Fig. 1. Illustration of the chicken-and-egg loop for circuit signoff with EM and AVS to compensate for performance degradation due to BTI.

In this work, we study the effects of EM on both signal and power/ground interconnects using recent models [21]. We quantify impact on circuit performance, power and lifetime in a system that uses AVS. We empirically demonstrate that EM-awareness can change power and area tradeoffs when designers choose corners for AVS signoff. Furthermore,

we demonstrate that different AVS strategies have different impacts on EM lifetimes. We conduct our experiments with a 28*nm* FDSOI foundry technology and commercial tool flows.

Our contributions are summarized as follows.

(1) We analyze interactions between EM degradation, and AVS signoff and scheduling, in a 28*nm* foundry FDSOI technology using commercial EDA tool flows. We address the three-way interactions between EM, BTI and AVS, and demonstrate that these interactions are significant at 28*nm* and beyond.
(2) We study the incremental cost of design to prevent EM relative to ignoring EM at signoff. We perform our analyses, with both modeling as well as ignoring of AVS signoff and scheduling.
(3) We demonstrate that the inaccuracy (penalty) of EM lifetime due to improper guardband against BTI at signoff can be as high as 30% in a 28*nm* technology. Furthermore, we demonstrate that choice of AVS voltage step size and scheduling strategies can result in up to 1.5 years of decreased EM lifetime.
(4) We provide signoff guidelines which suggest that the EM lifetime penalty can be compensated by paying an area penalty of up to 1.6% and a power penalty of up to 6%.

The remainder of the paper is organized as follows. In Section II, we review related works on AVS and EM signoff. In Section III, we study implications of a recent statistical EM model in AVS systems, and in Section IV, we describe our design of experiments and present results. In Section V, we describe future works and conclude the paper.

II. Related Works on AVS signoff

Several previous works address different aspects of EM. We taxonomize these works into three categories.

(a) Models for lifetime and wire degradation due to EM. Black proposes an empirical mean time to failure (MTTF) model of wires [6], which is the well-known Black's Equation. Arnaud et al. [4] and Federspiel et al. [11] study the failure processes in copper wires and extend Black's Equation. While previous works focused on developing physical models, Mishra et al. [21] propose a statistical model of the process of EM degradation. They demonstrate that their modeling approach can reduce the pessimism in Black's Equation-based EM signoff criteria.

(b) Approaches for EM evaluation and signoff. EM evaluations and optimizations in EDA tools rely on CPU-intensive computations and layout optimizations to constrain current densities that satisfy EM lifetime requirements. [28] [38] [36]. As technology advances, more physical design factors such as temperature [10], process variation [24], and growing dominance of BTI and AVS must be considered in order to achieve accurate EM evaluation and signoff.

(c) Physical design approaches for EM-durable circuits. In this category, we include wire-sizing and wire segmentation methods for the design of EM-durable circuits. Adler et al. [1] [2], Jiang et al. [12], Lienig et al. [19] and Yan et al. [26] develop wire-sizing algorithms for current-aware routers that avoid high current densities in circuits. They guarantee lifetime by ensuring that their algorithms always deliver current densities that are within the limits specified in technology files. Li et al. [18] develop wire segmentation and via insertion algorithms to create immortal wires by constraining interconnect segment lengths to be less than the Blech length [18].

Previous works on BTI in AVS systems [5] [9] [15] [16] [17] [20] [23] focus on the interactions between behaviors of AVS and BTI while ignoring EM degradation. Recently, Chan et al. [8] study signoff strategies that consider interactions between AVS and BTI, but do not consider EM in their work.

Our work falls at the intersection of categories (b) and (c), building on that of [8]. We consider EM signoff strategies in the presence of BTI and AVS, and we investigate approaches to the design of EM-durable circuits. To the best of our knowledge, we are the first to address the three-way interactions between EM, BTI and AVS, and to demonstrate that these interactions are significant at 28*nm* and beyond.

III. Implications of a recent statistical EM Model

We now study the implications of a recent statistical EM model [21] on system performance. The model is a function of wire geometry, electric field due to the supply voltage V_{DD}, and ambient temperature, and estimates degradation due to increased resistance on wires. We first verify correctness of the model in a 28*nm* foundry FDSOI technology and then quantify the delay impact due to EM on AVS systems. In our evaluations in Section IV, we use both the statistical as well as the traditional lifetime model using Black's Equation [6].

A. Characterization of EM Model

In previous works, such as [4] and [11], circuit measurements and empirical models demonstrate that the failure of wires due to EM has two stages. In the first stage (nucleation), height of void is less than the thickness of copper layer, so the wire resistance does not change significantly. Once the void occupies the whole cross-section of the wire, the degradation enters the second stage (growth) and the resistance of the wire suddenly jumps since the liner layer (tantalum), which has relatively higher resistance than copper, below the copper layer becomes the only conducting path in the void region. The jump in resistance occurs when the void height reaches the thickness of the copper layer. After this, the resistance increases linearly and finally causes defects in the wire. We model the time to reach the growth stage and the corresponding void lengths as random variables. We then apply the model in [21] to evaluate the impact of EM on circuit performance.

We use similar EM parameters as in [21] and apply the model to a 28*nm* technology BEOL process with W = 100*nm* (2X minimum width to avoid pessimism) and L = 150μm. Table I summarizes all the parameters that we use, as confirmed with [22]. The simulation results of ΔR due to EM are shown in Figure 2. When the current density is

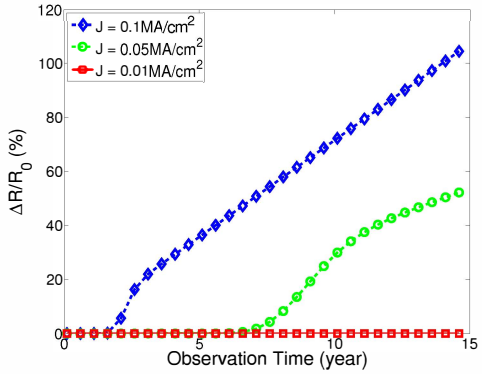


Fig. 2. Interconnect resistance increase in percentage due to different current densities in 28*nm* BEOL technology.

TABLE I
EM AND BEOL PARAMETERS.

	Definition	Value	Units
ρ_{Cu}	Resistivity of copper	2.50×10^{-8}	Ω/m
ρ_{Ta}	Resistivity of Tantalum liner	3.10×10^{-7}	Ω/m
T	Temperature	125	°C
σ_c	Effective critical stress for void nucleation	4.10×10^{7}	Pa
σ_{th}	Threshold for thermal stress	0	Pa
Z^*_{eff}	Effective charge number	5	
D_0	Diffusivity constant in Arrhenius' relation	9.80×10^{-9}	m^2/sec
k_B	Boltzmann constant	1.38×10^{-23}	J/K
e	Charge of single electron	1.60×10^{-19}	C
Ω_{Cu}	Atomic volume of copper	1.18×10^{-29}	m^3
B	Effective bulk modulus	10^9	Pa
μ_{Ea}	Mean of activation energy	7.52×10^{-20}	J
σ_{Ea}	Standard deviation of activation energy	8.00×10^{-22}	J
W	Copper wire width	100	nm
L	Copper wire length	150	μm
T_{wire}	Thickness of (Cu + Ta)	100	nm
T_{Ta}	Thickness of Ta	5	nm

low ($0.01MA/cm^2$), then the wire is immortal because the process of nucleation is too slow to form voids in copper wires. When the current density is high ($0.1MA/cm^2$), the process of nucleation is fast, and the resistivity increases rapidly and results in significant delay degradation. When the current density is in between the low and high values ($0.05MA/cm^2$), nucleation starts later than, but degrades at a similar rate as, when the current density is $0.1MA/cm^2$.

B. Impact of EM-Induced Performance Degradation in AVS Systems

We now assess the impact of EM degradation on wires for logic and clock signals and for power and ground distribution.

Impact on EM stress on signal wires. To evaluate the impact of EM-induced resistance increase (ΔR) from its initial resistance R_0 on circuits, we use Synopsys *HSPICE* to simulate a 30-stage chain of buffers in a 28*nm* FDSOI foundry technology library. In Figure 3, we simulate delay of the buffer chain[1] due to increase in resistance because of EM. We vary resistance from the nominal resistance of the wire[2] to 556% of the nominal resistance. We use multiple fanout-of-four (FO4) capacitive loadings, that is, we multiply the FO4 capacitive load by factors $\{1.0\times, 1.6\times, 2.1\times\}$. EM stress slows down circuit performance by increasing stage delay and by decreasing drive current due to increased output transition times.

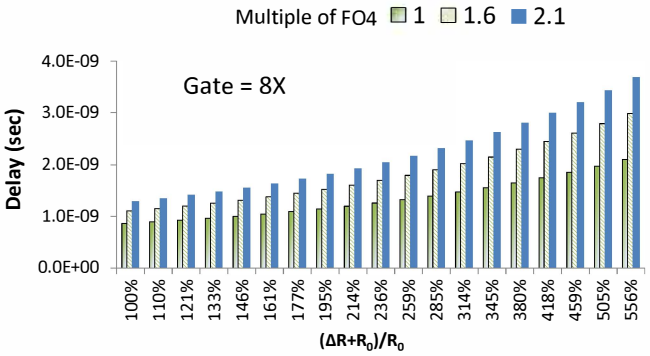


Fig. 3. Impact of ΔR on path delay with different capacitive loadings. V_{DD} = 1.1V.

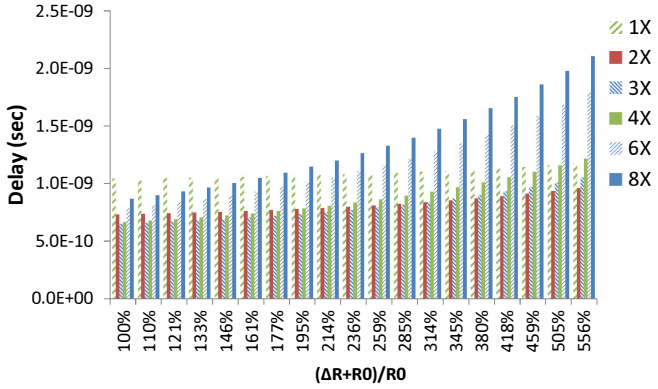


Fig. 4. Impact of ΔR on path delay due to EM stress with different gate sizes. V_{DD} = 1.1V.

We also study the impact of different gate sizes other than the 8× of the minimum-sized buffer to evaluate the impact of ΔR after gate sizing. For the delay shown in Figure 4, we observe that larger gates do not necessarily help to reduce the impact of ΔR. The possible reason is that the drive current of larger gates cannot compensate the increase in gate capacitance from the next stage. As we size up all the cells at the same time, so the capacitive load due to large input capacitances of large-sized gates also increase. The experiments above indicate that for typical signal wires, the model from [21] estimates that delay increases by ∼8% through cell chains with buffers smaller than 4× the minimum-sized buffer, when the wire resistance increases to high values (∼146%). According to our evaluation in Figure 2, this is equivalent to 10 years' degradation when the current density is $0.1MA/cm^2$.

[1]To consider the worst-case loading, we set the nominal buffer size to 8× the minimum-sized buffer from the 28*nm* FDSOI library.

[2]We assume the nominal wire resistance to be 600Ω, which is extracted from 28*nm* BEOL technology with L = 150μm and W = 50*nm*.

Impact of EM stress on IR drop on power and ground mesh. We use the circuit shown in Figure 5 to study the IR drop impact of EM stress on power and ground mesh. We define the supply voltage used by the core logic as V_{DD} and the voltage applied on the power and ground mesh (P/G mesh) and power ring by the regulator as $V_{regulator}$. When the resistance of the P/G mesh (R_{PG}) increases due to EM, the power consumed by the mesh increases when the drive current remains the same so as to achieve the same performance. However, the degradation of P/G mesh depends on scheduling of the supply voltage to compensate IR drop and BTI effects. Since different guardbands for BTI at signoff can change the behavior of voltage scheduling, the impact of EM on P/G mesh also changes with different guardbands.

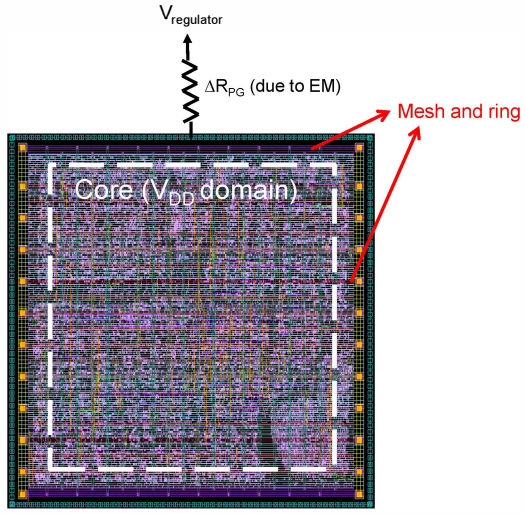


Fig. 5. Illustration of P/G mesh, V_{DD}, and $V_{regulator}$.

TABLE II
SIGNOFF CORNERS FOR BTI. V_{min}=0.90V, AND V_{max}=1.10V.

	Implementation #							
	1	2	3	4	5	6	7	8
V_{lib}	V_{min}	V_{min}	V_{max}	V_{min}	0.98V	0.97V	0.96V	0.95V
V_{BTI}	V_{min}	V_{max}	V_{max}	N/A	0.98V	0.97V	0.96V	0.95V

We choose eight different signoff corners defined by different V_{BTI} and V_{lib} [8] as shown in Table II to evaluate the impact on different-aged AES [37] implementations.[3] From [8], we estimate the final AVS voltage V_{final}, as obtained from cell chain simulations, to be 0.98V. Therefore, we sweep V_{DD} across {0.98V, 0.97V, 0.96V, 0.95V} to cover different margins for our AVS simulations. With the libraries characterized at the eight signoff corners, we perform synthesis, place and route (SP&R) and sign off the implementations with *Synopsys PrimeTime vH-2013.06-SP2* [32]. We report core power (defined as the power consumed by the design other than P/G mesh) as well as the P/G power. We account for EM stress and perform AVS simulations in *Matlab* [29] and calculate the core power by interpolating power simulation results obtained from *PrimeTime*.

We calculate the P/G mesh power by obtaining the initial R_{PG} = 2Ω from 28*nm* FDSOI BEOL foundry technology library, and the increase of wire resistance is modeled using the statistical EM model in [21]. We obtain the average current on the P/G mesh to be 10*mA* from our SP&R implementation and power simulations of the design AES. The calculated P/G power with the above assumptions are shown in Figure 6. When there is EM stress, the statistical model predicts a ∼1% power increase due to worst-case BTI degradation (Implementation #2). In summary, our experimental results with the statistical model in [21] indicate that it is optimistic with respect to the amount of EM degradation, leading to smaller estimated delay and power penalties. Therefore, we use both this model as well as Black's Equation in our further studies.

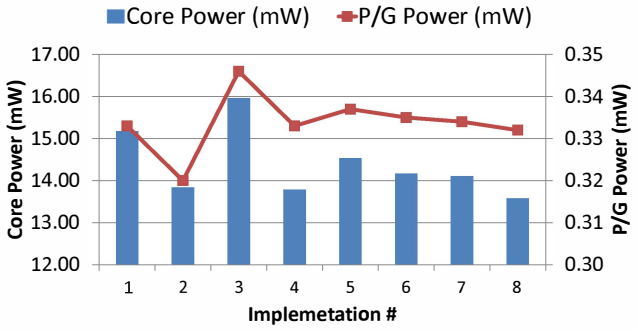


Fig. 6. Power comparison between different signoff corners with EM stress $\Delta R_{PG} > 0$.

IV. EXPERIMENTAL SETUP AND RESULTS

Our studies in Section III-B indicate that cell chains with buffers or inverters of different sizes have different behaviors due to EM stress. This relationship between gate sizes and EM vulnerability can lead circuit designers to change the *wire and gate widths* to build more reliable circuits when both EM and BTI can degrade the circuits.

In this section, we report experiments aimed at quantifying design costs in terms of power, lifetime and area of the implemented circuits. Total power changes with voltage scheduling due to AVS as well as due to effects of both EM and BTI, We use the following steps to implement our test circuits and evaluate design costs.

(1) We use Synopsys *SiliconSmart v2013.06-SP1* [35] to re-characterize the 28*nm* FDSOI library at different supply voltage V_{DD} and ΔV_{th} to obtain the impact of BTI on delay, dynamic power, and leakage power. We characterize a total of 48 libraries by setting V_{DD} to {0.9V, 1.0V, 1.1V}, threshold voltage of the PMOS V_{thp} to {0mV, 40mV, 80mV, 110mV}, and threshold voltage of the NMOS V_{thn} to {0mV, 20mV, 40mV, 55mV}.

[3]Implementation #4 has no BTI degradation in the signoff libraries, so V_{BTI} is not applicable.

(2) To compare the impact with different aging due to BTI, the circuits are synthesized, placed, and routed at eight different corners shown in Table II. We use Synopsys *Design Compiler vH-2013.03-SP3* [33] and Synopsys *IC Compiler vI-2013.12-SP1* [34] in the flow.
(3) The timing, dynamic power, and leakage power of the implemented circuits are measured using the 48 libraries, characterized above, with Synopsys *PrimeTime vH-2013.06-SP2* [32].
(4) The behaviors of AVS, BTI degradation, and EM degradation are simulated in *Matlab* [29]. The BTI analytical model is from [25] and calibrated to the data in [27]. For each time step, the circuit power, delay, and the wire degradation due to EM are updated using the two models. When the V_{DD} and ΔV_{th} are not exactly the same as the 48 data points in the previous step, we use interpolation to calculate the values.

We conduct the following three experiments.

- **Experiment 1.** The goal is to demonstrate the impact of final AVS voltage on EM lifetime.
- **Experiment 2.** The goal is to quantify the design costs to fix EM in systems with AVS.
- **Experiment 3.** The goal is to demonstrate the impact of voltage step size and scheduling due to AVS on EM lifetime.

A. Experiment 1 Results

We study impact on EM lifetime of the final AVS voltage by using the following steps.

- Step 1. Assume all the circuits have an initial lifetime of 10 years at a nominal voltage of 0.90V.
- Step 2. For each AVS timestep i, the remaining lifetime is calculated as follows [6] [13].

$$MTTF(i) = MTTF(i-1) \times \left(\frac{V_{DD}(i-1)}{V_{DD}(i)} \right)^2 \quad (1)$$

- Step 3. Update the lifetime after each AVS timestep until all the lifetime is used up.

Figure 7 shows how the final AVS voltage V_{final} affects EM lifetime for eight implementations of the AES [37] design. EM lifetime decreases for implementation #3 more than others because implementation #3 has large negative slack at signoff, hence higher V_{DD} is required to compensate for the negative slack. The degradation for implementation #3 is 30% of its lifetime, that is, decrease from 10 years to seven years. We notice that implementation #3 has obviously lower lifetime ($>$ one year) compared to #1 even though implementation #1 and #3 have similar V_{final} (difference $<$ $50mV$). The reason is that implementation #3 increases the V_{DD} very early due to less margin for BTI, so it degrades EM lifetime sooner than implementation #1. This figure demonstrates how AVS impacts EM lifetime and thereby EM signoff. We further study the impact of voltage scheduling on EM lifetime in Experiment 3.

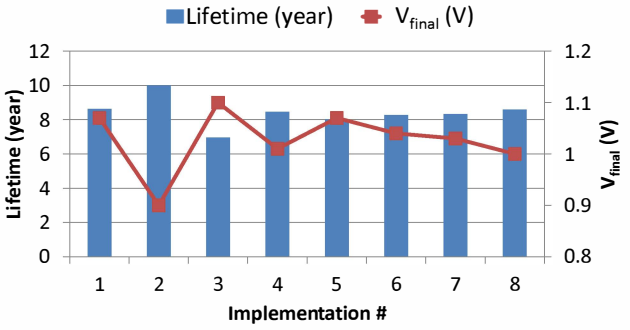


Fig. 7. Lifetime and V_{final} of the eight implementations of the AES design.

B. Experiment 2 Results

To quantify design costs due to fixing EM, we implement two designs AES and DMA, and perform gate-sizing for timing closure in Synopsys *IC Compiler* before signoff. We then apply EM constraints in an ALF file to the test circuits and use the following steps to fix the violations.

(1) Step 1. Generate initial EM violation report of wires with the EM constraints.
(2) Step 2. For each wire segment that has EM violation, use NDRs to fix EM violations.
(3) Step 3. Repeat Steps 1 and 2 until EM violations are fixed.
(4) Step 4. Re-route and apply gate-sizing to fix the remaining EM violations, if any and then perform timing recovery to fix all setup and hold time violations.[4]

Figures 8 and 9 respectively show power and area for the AES and DMA designs across eight implementations in Table II, and for three cases: (i) BTI signoff is not aware of EM, (ii) BTI signoff is EM-aware and uses the traditional Black's Equation model, and (iii) BTI signoff is EM-aware and uses the recent statistical EM model. As demonstrated in Section III, the statistical EM model is optimistic and has almost same power as case (i) for most implementations. EM-awareness decreases power in AES for implementations #1 and #2 due to downsizing of gates and constraining max fanout in the clock network. In DMA, EM-awareness increases area per the statistical model because of resistance increase and addition of smaller buffers to fix setup violations. The worst-case area penalty ($\sim$1.6%) is for implementation #2 of DMA, and the worst-case power penalty ($\sim$6%) is for implementation #6 of AES.

C. Experiment 3 Results

EM lifetime is affected due to voltage scheduling in systems using AVS. We use five different voltage schedules S1–S5. The initial voltage for all these schedules is 0.90V.

[4]Note that the baseline signoff corner is set at V_{DD} = 0.9V. We do not guardband BTI at signoff in this experiment, and assume AVS will be used to compensate the aging. Since we size down cells to fix EM violations, the circuit timing will be affected.

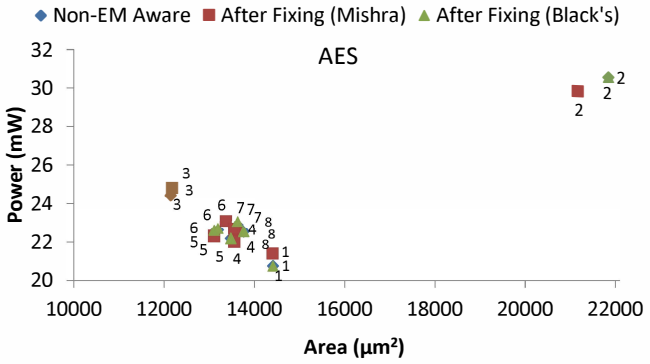


Fig. 8. Power and area due to EM fixes on AVS systems using both Black's Equation and [21] models for the AES design.

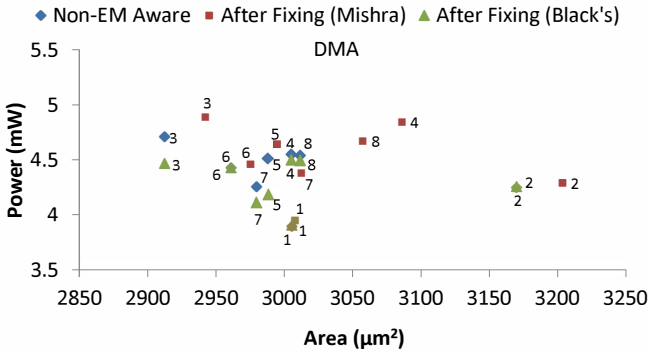
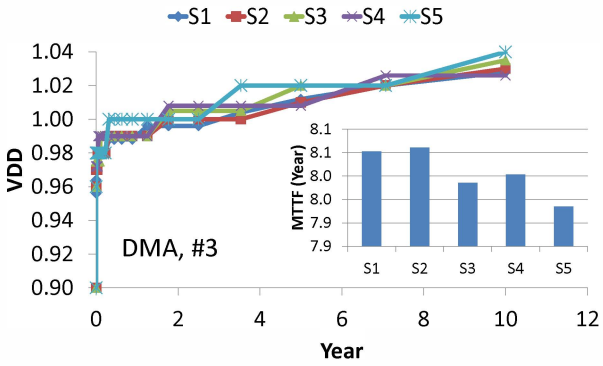


Fig. 9. Power and area due to EM fixes on AVS systems using both Black's Equation and [21] models for the DMA design.

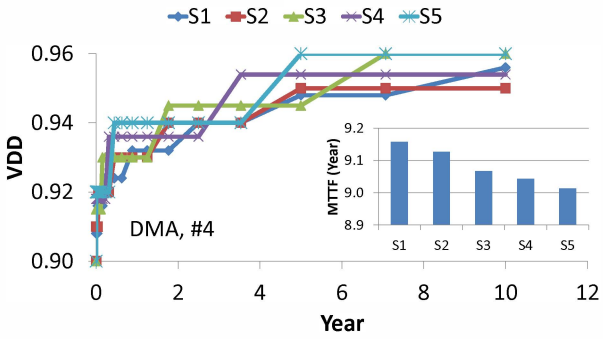
The steps by which each schedule is increased is shown as the tuple (schedule, voltage step): (S1, 8mV), (S2, 10mV), (S3, 15mV), (S4, 18mV) and (S5, 20mV), The voltage step is made whenever delay is higher than target due to EM degradation. We conduct the experiment as follows.

- Step 1. Signoff the AES and DMA designs at 0.90V with no guardband for EM and assume that AVS will compensate aging due to BTI.
- Step 2. Simulate the delay degradation with BTI [25] and EM [21] models. To compensate delay degradation, increase the supply voltage V_{DD} to a higher value in each timestep according to the schedule that is being used.
- Step 3. Update remaining lifetime using Equation (1) and repeat Steps 1 and 2 until the entire lifetime is consumed.

Figures 10(a) and (b) show the EM lifetime for the five schedules for the DMA design. Figures 11(a) and (b) show the EM lifetime for the five schedules for the AES design. Implementation #4 is the baseline with no BTI degradation. We observe that a scheduling with voltage steps of $18mV$ or $20mV$ can result in up to 1.5 years of decreased EM lifetime, which indicates that small fluctuations in guardband can result in significant lifetime change due to different voltage scheduling requirements.



(a)

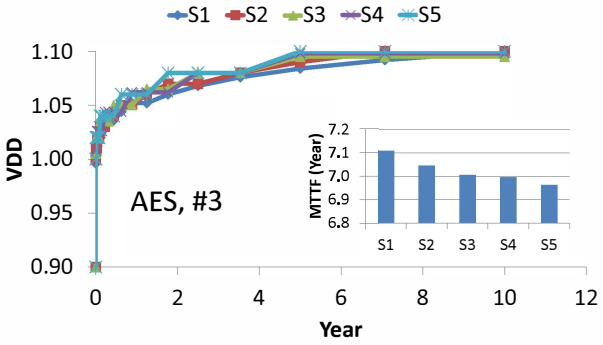


(b)

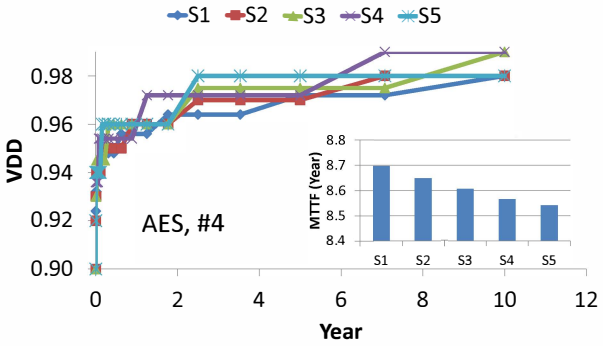
Fig. 10. Impact on EM lifetime due to five different voltage schedules in AVS systems for DMA implementations (a) #3 and (b) #4.

V. Conclusions

Reliability signoff affects circuit performance, power and lifetime. In this work, we study the joint impact of BTI, AVS and EM on signoff. We use a statistical EM model recently proposed by [21] and apply it to our AVS simulations to study the signoff of both EM and BTI. We use two EM models, (i) resistance increase as predicted by the model in [21] in AVS systems, and (ii) the traditional Black's Equation-based EM model; fixes are implemented in commercial tool flows, and EM constraints are from a 28*nm* FDSOI foundry library. The model from [21] is easier to apply in earlier implementation stage by derating the resistance in commercial tools, but it tends to be optimistic in our characterization. Our experimental results indicate that for signal wires, large drivers should be avoided as they suffer from more delay degradation due to EM-induced resistance increase. For P/G mesh, we quantify the impact of resistance increase and conclude that the area-power curve formed by different BTI signoff corners is shifted due to EM. We empirically analyze the cost of fixing EM at signoff with different guardbands against BTI. In our studies, this cost is up to 1.6% increase in area and 6% increase in power. Our ongoing work seeks to (i) explore signoff methodologies for other reliability mechanisms at advanced foundry nodes, (ii) improve accuracy of signoff by considering thermal gradient effects, and (iii) develop a learning-based modeling approach to quantify design costs of reliability.



(a)



(b)

Fig. 11. Impact on EM lifetime due to five different voltage schedules in AVS systems for AES implementations (a) #3 and (b) #4.

ACKNOWLEDGMENTS

We thank Mr. Vivek Mishra and Professor Sachin Sapatnekar for their very helpful clarifications regarding the EM model described in their work [21].

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