Mission Profile Aware IC Design – A Case Study

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***Abstract*—Consistent consideration of mission profiles throughout a supply chain is essential for the development of robust electronic components. Consideration of mission profiles is still mainly a manual task today despite rapidly decreasing robustness margins in modern automotive semiconductor technologies. Mission profile awareness aids the automation of robustness aware design by formalizing and partially automating the generation, transformation, propagation and usage of all component-specific functional loads and environmental conditions for design implementation and validation. In addition, it aids the development of electronic components in yet immature technologies or in technologies with tight parameter variation bounds. This paper introduces the general concept, requirements and context of mission profile aware design. The general design approach is presented along with key differences and enhancements to existing design approaches. A case study focusing on mission profile usage and electromigration failure avoidance is presented to demonstrate various aspects of mission profile aware design.**

***Keywords*—Electromigration, IC Design, Mission Profile, Mission Profile Aware Design, Reliability, Robustness, Validation, Verification**

I. Introduction

When new semiconductor technologies were developed in the past, they would typically undergo a five-year maturing period in the consumer sector before being introduced to automotive electronics. However, the increasing demand for high performance automotive components, along with severe cost pressures, now result in a significant shortening of the allowed maturing time (see Fig. 1).

For conventional automotive Smart Power [1] and high-voltage semiconductors Moore's Law is presumably coming to an end within the next decade. The trend lines of Smart Power and high-voltage semiconductor technologies in Fig. 1 are decreasing significantly slower than the trend line for leading-edge CMOS logic. Application-specific requirements and design productivity are clearly apparent as key drivers that will influence future semiconductor trends from a system-level perspective in automotive electronics.

Today's leading-edge automotive semiconductor technologies are challenged by very high robustness requirements of electronic systems, modules (e.g., electronic control units) and their individual electronic components (henceforth, "components"). Such components are typically operated under very harsh environmental conditions and in the steady presence of high temperatures, high voltages and large current flows. These unfortunate conditions also become increasingly relevant to non-automotive and consumer oriented semiconductor applications as their manufacturing technologies continue to downscale.

The current ITRS roadmap lists several so-called "red brick" problems, such as electromigration and electric field related stress, for which no feasible mid- and long-term solutions are known today [2]–[4]. A feasible approach to mitigate these and other reliability problems is to reduce or even to eliminate the design uncertainty that exists in today's supply chain. Typically, main contributors of this uncertainty include missing technology characterization data (e.g., failure models and parameter variations), non-formalized environmental stress conditions and functional loads, inconsistent design data flows, as well as limited robustness awareness of EDA tools.

As a consequence, the robustness of components must be considered as a design target in order to benefit from modern automotive semiconductor technologies. This necessitates the consistent consideration of all relevant environmental conditions and functional loads each electronic system, module and component has to sustain during manufacturing, assembly, storage and operation. These loads and conditions are formalized in so-called "mission profiles" [5]–[7].

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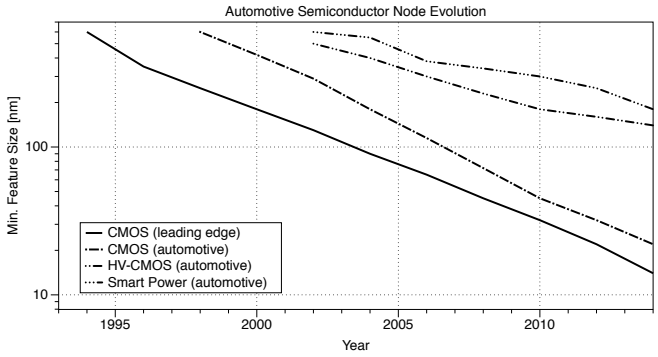

Fig. 1: Technology node evolution of several automotive semiconductor technology classes [2].

A mission profile defines all operating conditions for an electronic system, module or component in the intended target application. The consistent usage of mission profiles allows an early and precise identification of robustness limiting factors and mechanisms with regard to functional and parametric robustness as well as to reliability. For components, this includes the identification of dominant failure mechanisms, such as corrosion, electromigration (EM), hot carrier injection (HCI), negative/positive bias temperature instability (NBTI, PBTI), stress voiding (SV), time-dependent dielectric breakdown (TDDB) and others. In addition, functional and parametric robustness require the worst-case distance (WCD) and spread of performance parameters to be considered with respect to the specification [8].

This paper outlines the core concepts of mission profile aware design. Mission profile aware design provides automation for substantial parts of the robustness validation flow [5]–[7] by formalizing the generation, transformation, propagation and usage of mission profiles for the design implementation and validation of modules and components at each stage in the supply chain. In addition, it also formalizes and improves the communication flow within the supply chain. Mission profile aware design thereby reduces the design uncertainty and aids the development of components in yet immature technologies or in technologies with tight parameter variation bounds. Furthermore, it aids the decision process during reliability budgeting, and it addresses the traceability requirements for automotive electronic component designs according to ISO 26262 [9].

Mission profile aware design represents a generic design approach, and hence, it is not restricted to automotive applications. The usage of mission profiles has also a significant impact on module and component designs in various other fields, such as industry applications [10], renewable energy systems [11]–[13], and aerospace systems [14].

The remainder of this paper is structured as follows. Section II introduces and discusses the motivation and core concepts of a mission profile aware design flow. A case study focusing on mission profile usage and electromigration failure avoidance is presented and discussed in Section III. Finally, Section IV provides the summary and conclusions.

II. Mission Profile Aware Design

A. Motivation and Related Work

Electrical/electronic modules and components are subjected to various stress conditions during their manufacturing, assembly, storage and operation. These stress conditions arise from their ambient environment (e.g., ambient and operating temperatures, humidity, mechanical vibration, etc.), as well as from their functional loads (e.g., electrical potentials and currents, thermal heat flows, etc.) due to module and component operation.

These conditions contribute to various physical and chemical processes, i.e., failure mechanisms, that can degrade the functionality of a module/component or even permanently damage it over time. At the module level, dominant failure mechanisms may include solder joint EM, metal ion migration, whisker growth, metal fatigue and others [7]; mechanisms at the semiconductor level include corrosion, EM, NBTI, PBTI, TDDB, SV and others [15], [16].

All relevant, i.e., dominant, failure mechanisms must be considered by applying reliability engineering methods during the development of any module and any component in order to guarantee their robustness. This includes methods to prevent the likelihood or frequency of failures, to identify the root cause of failures, to master failures that do occur, and to estimate the reliability of designs based on available design data, time-to-failure models and measured reliability data of manufactured test components [15], [17].

A formalized approach to evaluate the robustness of modules and components is the so-called "robustness validation" process. Robustness validation is defined as an approach with which the robustness of a component to the environmental and loading conditions (mission profile) of an electrical or mechanical application is proven, and focused assertions regarding its reliability can be made [5]. While robustness validation is mainly driven by the automotive industry, its impact extends far beyond the automotive world. General robustness validation guidelines were recently published for semiconductor and MEMS components [5], [6], and electrical/electronic modules [7].

As stated before, robustness validation and mission profile consideration is still a mainly manual task today. On one hand this is attributed to a missing mission profile content and format standardization. This increases design uncertainty considerably, and hence, may also lead to over- and under-design at each stage in the supply chain. On the other hand, design flows, tools and methodologies within the supply chain are very heterogeneous and often incompatible with each other. This often prevents critical design information to be available when needed and in the quality that is needed. Additionally, the vast majority of EDA tools is currently not aware of mission profiles, thus leaving the dimensioning and validation task entirely in the hands of designers.

A mission profile aware design flow must allow reliability engineering and robustness validation to be applied consistently and efficiently within the entire supply chain. This requires

- a standardization of the mission profile content and format,
- methods to derive initial mission profiles and to transform them into component-specific mission profiles,
- interfaces of EDA tools to access mission profile information,
- models and methods to calculate the effective lifetime of components for dominant failure mechanisms,
- methods to convert dynamic transient loads to static loads,
- methods to calculate the functional and parametric robustness,
- procedures to distribute transformed mission profiles to the next lower level in the supply chain,
- procedures to back-annotate robustness information to the next higher level in the supply chain, and
- means to provide vendor-specific IP protection.

The following subsections introduce and discuss the concept of mission profile aware design, its core components, as well as various design flow aspects.

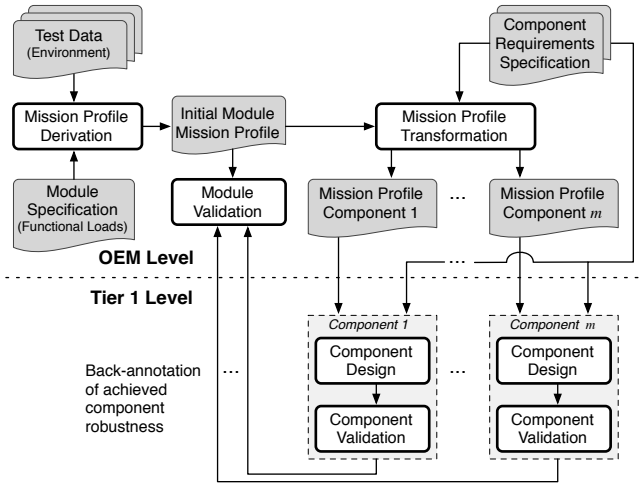

Fig. 2: Mission profile aware design flow for one electric/electronic module at OEM level and m components at Tier 1 level.

B. Mission Profile Documents

As mentioned before, a mission profile comprises all information about environmental conditions and functional loads of a module or component. By definition, any mission profile is specific to the corresponding module or component. This is regardless of the type of module or component. The structure of a generic mission profile document is given here as:

- Document root
  - Document header
  - Operating state definition
  - Component definition
    - Port definition
      - Operating state dep. functional loads
    - Property definition
  - Back-annotation data

The document header contains, at a minimum, information about the creator, details of the (transformation) methods used to create the mission profile, a document derivation history, a document version and a unique identifier to guarantee document traceability.

The operating state definition section defines all states of the module/component manufacturing, assembly, storage and operation (e.g. storage, sleep, wake-up, high-speed operation, low-speed operation, cool-down, etc.). The state definition includes all states of regular and special operation, but excludes states of intentional or unintentional misuse. Each state is hereby referenced by a unique identifier, the environmental conditions such as the average operating temperature or average humidity, and the accumulated duration the module/component is intended to spend in this operating state.

The component definition section contains the description of the module/component itself. Here, the component type (e.g., electronic control unit (ECU), printed circuit board, discrete capacitor, sensor, IC, etc.) and corresponding module/component properties (e.g., ECU case temperature or max. IC junction temperature, etc.) are defined. Furthermore, all physical and electrical input and output ports are uniquely defined. Functional loads, such as an electrical current or a thermal heat flow, are linked with an operating state and assigned to a unique module/component port.

Finally, the back-annotation section contains information about the achieved and proven robustness of the individual module or component (see Fig. 2). This includes the worst-case distance (WCD) and spread of performance parameters with regard to the specification (functional and parametric robustness) [8]. In addition, it also includes the so-called "Robustness Indication Figure" (RIF) values of the most critical failure mechanisms in the module or component [5]–[7].

C. Design Flow and Flow Components

The generic mission profile aware design flow and its components are depicted in Fig. 2. The flow originates from the top-level module (e.g., ECU) at OEM level and traverses down to all subcomponents at the Tier n level (e.g., ICs, passive components, mech. parts, etc.).

An initial mission profile is derived for the top-level module based on test data. Test data is typically obtained from detailed measurements of environmental stress conditions, such as transient temperature, humidity or vibration profiles. While there exist general guidelines on how to derive the initial system mission profile [7], no formalized and automated procedure has yet been defined. Thus, the generation and tailoring of an initial mission profile still remains the specific know-how of system/module design houses. This is despite established approaches, such as scenario based and multi-corner multi-mode (MCMM) based design. The module designer then adds the functional load conditions, such as electrical currents or potentials, to the initial system mission profile (see Section II-B). These conditions are typically directly derived from the system or module specification or from system-level and component-level simulation results.

The initial mission profile of the top-level module is then transformed into several component-specific mission profiles, one for each component. The transformation step converts the global conditions, i.e., environment and functional loads, from the module level to the local component level. For example, the temperature profile of an ECU is shifted by a positive temperature offset when it is converted to the local temperature profile of an IC component. This is due to the thermal impedances of the IC and its package, which cause the level of an IC's junction temperature profile to be higher than the average temperature of the upper-level ECU module. The transformation itself is specific to the physical structure, design and intended function of the component.

The component-specific mission profile is then used for design implementation, verification and validation of the component. Validation hereby defines a set of tests and analyses to demonstrate that the module or component is suited for its intended use according to the given mission profile. In order to account for parametric and functional robustness of a module or component, its WCD parameters are calculated according to [8]. The RIF values of the module/component are calculated according to [5]–[7].

After completing the validation phase of a component, its validation results are then back-annotated to the next higher module level using the corresponding section in the mission profile document. A mission profile aware design flow must thus ensure that the back-annotation information of *all* components is correctly transferred to the next higher module level. These validation results are then used to calculate the robustness parameters of the module [8]. The transformation, design and validation process continues as long as subcomponents that can act as local top-level modules or components are available. In contrast to the implementation flow, the back-annotation flow is strictly bottom-up and may include design iterations.

D. Requirements

Time-to-failure models, such as Black's Law [18] or probabilistic models [19] for electromigration, or Coffin-Manson [20], [21] for metal fatigue, are required in order to calculate the component-specific RIF values of all critical failure mechanisms. All parameters of (dominating) time-to-failure reliability models are to be derived from accelerated lifetime experiments using manufactured test components or standard test structures. This is typically done as part of the mandatory technology characterization process [22]. The time acceleration is hereby directly dependent on the failure mechanism in focus [15]–[17]. This requires an in-depth understanding and assessment of all dominant physical and chemical processes acting within a component.

Time-to-failure models are used in conjunction with available functional load and design data to perform design verification and validation tasks, such as aging simulation for NBTI, HCI or TDDB

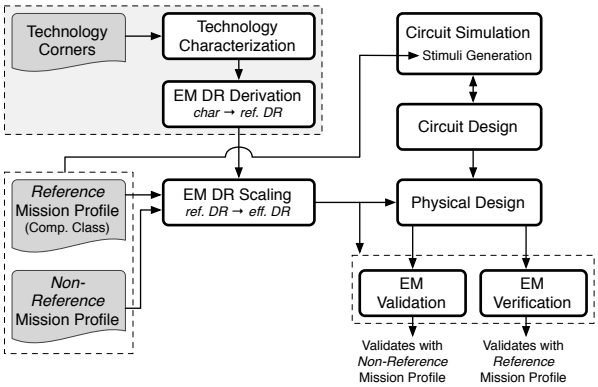

Fig. 3: Generic electromigration aware design flow.

(RelXpert [23], Eldo [24]) or current density verification [25], during the design phase. Additionally, preventive design measures must always be taken into consideration to account for insufficient reliability models, purely random errors or yet unknown failure mechanisms [9], [17].

Design environments within today's supply chain are very heterogeneous, and the flow of mission profile data is typically quite fragmented and unidirectional in these environments. As of today, major limitations exist due to missing mission profile format and content standardization. This effectively prevents disparate design flows of systems/modules and components from interacting effectively and efficiently with each other. Indeed, this obstacle is one of the primary reasons why EDA algorithms and tools are not yet aware of mission profiles. As a consequence, a mission profile standard, along with standardized tool APIs, are primary requirements to establish a mission profile aware design flow.

To fully establish a comprehensive mission profile aware design flow as outlined in Section II-A, further advances are required for (a) the systematic and data-driven generation of initial mission profiles, (b) their transformation into component-specific mission profiles, (c) the derivation of realistic simulation stimuli, (d) the establishment of standard mission profile data APIs for design tools and algorithms, and (e) studying the impact of component-specific mission profiles on reusability.

E. Characterization

The existing Design-For-Reliability approach primarily focuses on the individual module or component itself. While this clear separation between different design levels is desirable from a designer's point of view, it becomes increasingly difficult and even impossible to maintain, as noted above (see Section I). By contrast, mission profile aware design simultaneously focuses on all module and component levels – both global *and* local – in the design chain.

The bidirectional flow of mission profile data outlined in Section II-C formalizes, and thereby improves and accelerates in various ways, the communication between the design levels and design partners in the supply chain. Notably, the formalized back-annotation represents one of the major cornerstones of mission profile aware design, which enables early, fast and precise identification of robustness-critical components. To address today's and future design challenges [2], the Design-For-Reliability approach must thus evolve into a mission profile aware design approach by extending its currently locally-oriented focus to a more globally-oriented focus.

III. Case Study – Electromigration Aware Design

In this section, we present and discuss a small case study to demonstrate various aspects of mission profile aware design with respect to electromigration (EM). The EM aware IC design flow discussed below conforms to the definition of a mission profile aware design flow from Section II.

A. Electromigration Aware Design Flow

The generic EM aware design flow is depicted in Fig. 3. Its primary components are EM design rule derivation, EM design rule scaling, circuit design including simulation and EM aware physical design as well as EM verification and validation of the final layout.

Reference electromigration design rules (EM DR) are derived during the technology characterization phase based on accelerated EM stress tests [22], [26] (see Section III-B). A primary objective is here to derive current density design rules that allow scalability with regard to IC-specific EM target lifetime [27], operating temperatures and design complexity. These design rules are typically found in the design rule manual of an IC technology.

To improve applicability, standardized mission profiles are often used to account for various application classes such as consumer, automotive, industry, medical, and aerospace. The component-specific mission profile must be used for design implementation and validation of the IC in case it does not fit any of the available class-specific mission profiles. The reference design rules must be scaled in both cases according to the requirements of either the application class or the specific IC project (see Section III-C).

The operating state definitions of the mission profile and the specification requirements are used to derive a set of simulation stimuli for each operating state [8]. These stimuli are subsequently used to obtain all effective terminal currents within the electrical circuit for each operating state. These currents are then used during the IC physical design phase to lay out all interconnects with the correct cross-section areas, and to connect to all terminal pins without causing current density violations. The compliance with these EM design rules is then verified in the final layout result, using approaches such as [25] (see Section III-D).

A pure physical design validation with respect to EM is performed if the temperature profile or the duration of operating phases is modified while maintaining the physical layout. This results in new current density design rules that differ from the DRM reference design rules, and that must be obeyed by the physical design as a condition of validation. Electromigration validation is crucial for the reuse of physical layout. Due to space limitations, we subsequently focus on scalable current density design rules as the primary means to address EM within ICs.

B. Derivation of Reference Design Rules

Electromigration mean time-to-failure may be modeled according to Black's Law [18]:

$$t_{50} \;=\; \frac{A}{j^n} \cdot \exp\left[\frac{E_\mathrm{a}}{k_\mathrm{B} \cdot T}\right] \tag{1}$$

with t_{50} as the time when 50% of all interconnects have failed, j as current density in the interconnect metallization, E_a as layer-specific EM activation energy, n as dimension-less current density scaling factor, k_B as Boltzmann constant, T as interconnect temperature, and A as a cross-section dependent constant. The terms E_a, A and n are to be obtained during technology characterization [22], [26]. They must be monitored closely during manufacturing [26], [28]. The temperature T accounts for the environmental stress conditions defined in the mission profile, whereas j accounts for the functional load (electrical current) and for the physical design solution (cross-section area of the interconnect).

Since even a single damaged interconnect can cause the entire IC to fail, it is obvious that (1) cannot be used to describe the EM reliability target for an IC without further adjustments. In order to describe and define real component-specific EM design rule targets, (1) is rewritten as

$$t_{\mathrm{life,ref}} = AF_\mathrm{TF} \cdot AF_\mathrm{T} \cdot AF_\mathrm{q} \cdot t_{50,\mathrm{char}} \tag{2}$$

$$= AF_\mathrm{TF} \cdot AF_\mathrm{T} \cdot AF_\mathrm{q} \cdot \frac{A}{j_\mathrm{char}^n} \cdot \exp\left[\frac{E_\mathrm{a}}{k_\mathrm{B} \cdot T_\mathrm{char}}\right] \tag{3}$$

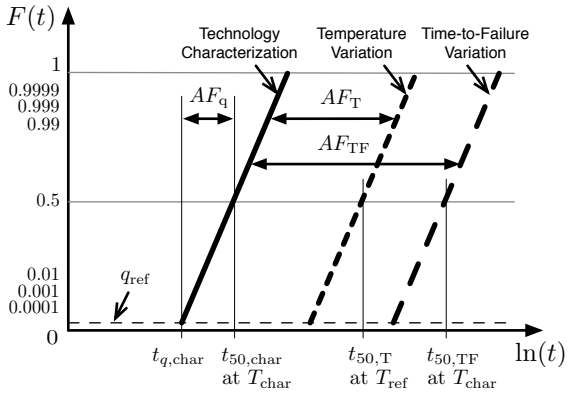

Fig. 4: EM lifetime scaling factors AF_TF, AF_T and AF_q, as well as $F(t)$ as cumulative failure probability and q_ref as error quantile.

with

$$AF_\mathrm{T}\left(T_\mathrm{ref}, T_\mathrm{char}\right) = \exp\left[\frac{E_\mathrm{a}}{n \cdot k_\mathrm{B}} \cdot \left(\frac{1}{T_\mathrm{ref}} - \frac{1}{T_\mathrm{char}}\right)\right] \tag{4}$$

$$AF_\mathrm{q}\left(0.5, q_\mathrm{ref}\right) = \frac{S_1}{\exp\left[\mathrm{norminv}(q_\mathrm{ref}) \cdot \sigma\right]} \tag{5}$$

and $t_{\mathrm{life,ref}}$ as the *targeted* reference lifetime when the cumulative fraction, i.e., a quantile q_ref, of interconnects is projected to fail while being subjected to a constant reference temperature T_ref and stressed with a reference current density j_ref. The term $t_{50,\mathrm{char}}$ denotes the time when 50% of interconnects have failed during characterization at temperature T_char while being stressed with the current density j_char. Scaling factors for target application lifetime, effective interconnect temperature and permissible failure rate are denoted as AF_TF, AF_T, AF_q (see Fig. 4). The target application lifetime factor AF_TF is used to tailor EM design rules to specific application requirements and optimization goals [4]. The lognormal standard deviation obtained from technology characterization is denoted as σ.

One has to consider $t_{\mathrm{life,ref}}$ as target lifetime, from which j_ref is finally derived. The target EM lifetime of an IC should not be confused with its cumulative EM operating lifetime $t_{\mathrm{life,eff}}$, which must be shorter than $t_{\mathrm{life,ref}}$ in order to fulfill the validation criteria (see Section III-C). It is the obvious from (2)–(5) that $t_{\mathrm{life,ref}}$ must increase proportionally with rising reliability requirements. This leads to several important implications for the final EM design rule derivation.

According to (5), the larger the number of interconnects in an IC, the smaller the error quantile q_ref must be chosen, which then results in a higher EM target lifetime $t_{\mathrm{life,ref}}$. This observation leads to the conclusion that reference current density design rules tailored for IC designs with millions of interconnects cannot be safely utilized for designs with billions of interconnects (see Section III-C for details).

The term S_1 in (5) accounts for the low confidence level during technology characterization. This is due to the fact that only a few hundred of interconnect structures can be efficiently characterized. The characterization result is then up-scaled to millions or even billions of interconnects in later applications. Hence, S_1 must be set to values larger than 1.0 to account for the low confidence level. Additionally, it is obvious from (4) that temperature scaling has a significant impact on the application reliability, and must thus being carefully considered during the layout implementation, verification and validation.

The layer-dependent reference current density j_ref at T_ref is finally derived from (2)–(5) as

$$j_\mathrm{ref}(T_\mathrm{ref}, q_\mathrm{ref}) = \frac{j_\mathrm{char}\left(T_\mathrm{char}\right)}{AF_\mathrm{T}\left(T_\mathrm{ref}, T_\mathrm{char}\right) \cdot AF_\mathrm{q}\left(0.5, q_\mathrm{ref}\right) \cdot AF_\mathrm{TF}} \tag{6}$$

C. Effective Design Rules based on Mission Profiles

For most applications the *reference* EM design rules must be scaled to component specific, i.e., *effective*, EM design rules to account for

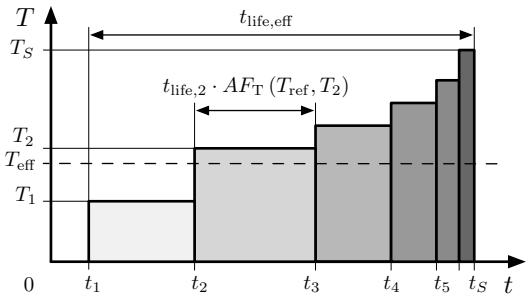

Fig. 5: Example of temperature vs. cumulated eff. lifetime profile.

the IC's real usage conditions as defined by its mission profile:

$$t_{\mathrm{life,ref}}(q_{\mathrm{ref}}) \rightarrow t_{\mathrm{life,eff}}(q_{\mathrm{eff}}) \tag{7}$$

$$T_{\mathrm{ref}} \rightarrow T_{\mathrm{eff}} \tag{8}$$

$$j_{\mathrm{ref}} \rightarrow j_{\mathrm{eff}} \tag{9}$$

The application-specific effective error quantile q_{eff} is calculated as:

$$q_{\mathrm{eff}} \ll \frac{1}{m} \tag{10}$$

where m is the number of interconnect segments in the IC. The term q_{eff} accounts for the IC complexity and the EM reliability budget.

Given a mission profile, the term T_{eff} represents the effective (design) temperature at which an arbitrary current flow causes the same cumulative EM damage as it would at T_{ref} with the reference mission profile. (The current flow itself is here considered to cause no significant self-heating in the interconnects.) One can calculate T_{eff} as follows:

$$\frac{1}{T_{\mathrm{eff}}} = \frac{1}{T_{\mathrm{ref}}} - \frac{k_{\mathrm{B}}}{E_{\mathrm{a}}} \cdot \ln\left(\frac{t_{\mathrm{life,eff}}}{t_{\mathrm{life,ref}}}\right) \tag{11}$$

with

$$t_{\mathrm{life,eff}} = \sum_{s=1}^{S}\left[t_{\mathrm{life},s} \cdot \exp\left[\frac{E_{\mathrm{a}}}{n \cdot k_{\mathrm{B}}} \cdot \left(\frac{1}{T_{\mathrm{ref}}} - \frac{1}{T_s}\right)\right]\right] \tag{12}$$

where T_s is average temperature at operating state s, $t_{\mathrm{life},s}$ is wall clock duration of s, $t_{\mathrm{life,eff}}$ is effective EM lifetime at T_{eff}, and $t_{\mathrm{life,ref}}$ is from (2) (see Fig. 5). In addition to its dependence on the application mission profile, T_{eff} also depends on the interconnect layer as seen in (3), (4) and (11). Hence, T_{eff} must be calculated separately for each interconnect layer of the technology, and the highest value is then used as the reference for physical layout and for current density verification and validation.

The mission profile-specific effective current density j_{eff} for each interconnect layer can now be calculated by reusing (4)–(6):

$$j_{\mathrm{eff}}\,(T_{\mathrm{eff}}, q_{\mathrm{eff}}) = \frac{j_{\mathrm{ref}}\,(T_{\mathrm{ref}})}{AF_{\mathrm{T}}\,(T_{\mathrm{ref}}, T_{\mathrm{eff}}) \cdot AF_{\mathrm{q}}\,(q_{\mathrm{ref}}, q_{\mathrm{eff}}) \cdot AF_{\mathrm{TF}}} \tag{13}$$

Finally, the Robustness Indicator Figure (RIF) defines the achieved robustness margin of the IC with respect to a specific failure mechanism – in this case, EM. While obeying a maximum current density j_{eff}, an obtained RIF value of $\gg 1.0$ then proves that the IC is qualified for its intended application. Given a target lifetime goal $t_{\mathrm{life,target}}$, the basic RIF value is then calculated according to [5]:

$$\mathrm{RIF} = \frac{t_{\mathrm{life,target}}}{t_{\mathrm{life,eff}}}\ . \tag{14}$$

D. Results

Two automotive IC designs *Design1* and *Design2* belonging to different application categories (motor management and passenger safety) have been used to demonstrate selected aspects of electromigration aware design. Both ICs were designed for the same semiconductor technology and same reference mission profile. A single non-reference mission profile was used to validate the IC designs for applications with longer power-on times in certain operating states. Furthermore, the sensitivity to current density criticality was investigated with respect to previous- and next-generation technology nodes.

The functional load at all circuit instance terminals was obtained via circuit simulation and subsequent current value propagation. The operating state-dependent transient current waveforms were post-processed for each terminal to derive effective scalar values for the EM-relevant average and RMS currents (dynamic stress → static stress conversion). Since full-chip simulation of these complex automotive mixed-signal ICs has not been feasible on the device-level, terminal currents at cell-pins of some IC blocks were automatically propagated to the top-level cell.

The effective EM design temperature T_{eff} and the corresponding j_{eff} were calculated using (11) and (13). First, the impact of the new mission profile on the number of current density-critical nets was evaluated (see Fig. 6). The new mission profile had only minor impact on *Design1*, but had a significant impact on *Design2* (see Figs. 6a and 6c). (The previous mission profile is denoted as "nom. temperature, min. Metal1 wire width"; the new mission profile with higher T_{eff} is denoted as "nom. temperature + 25K, min. Metal1 wire width".) Second, the current densities in the physical layout were calculated with [25] and compared with the permitted values of j_{eff}. Critical current density violations were confirmed for *Design2*, which did not validate for the new mission profile without further layout adjustments.

Both designs demonstrated a high sensitivity to current density criticality, as the number and percentage of critical nets increase dramatically in a next-generation technology node having smaller minimum feature sizes than the previous technology node. This high sensitivity demonstrates one of the primary reasons why automotive technologies are a very slow technology follower. However, the mission profile based approach outlined in this section significantly reduces the EM design uncertainty, which allows designers to consider technology and design limits deliberately, and more aggressively, without compromising (EM) reliability.

IV. Summary and Conclusions

In order to realize full benefit from modern semiconductor technologies, robustness must now be actively considered as a first-class design target. This includes the consistent consideration of all relevant environmental stress conditions and functional loads, which are formalized in mission profiles. In this paper, we have outlined the necessity and concept of mission profile aware design. Despite several open challenges, mission profile aware design represents a significant enhancement to the existing Design-For-Reliability approach by reducing design uncertainty in the supply chain. A case study focusing on mission profile usage and electromigration failure avoidance is presented to demonstrate various aspects of mission profile aware design. Future work must especially focus on the standardization of mission profiles, on the derivation and transformation of mission profiles, as well as on the consideration of mission profiles within EDA tools.

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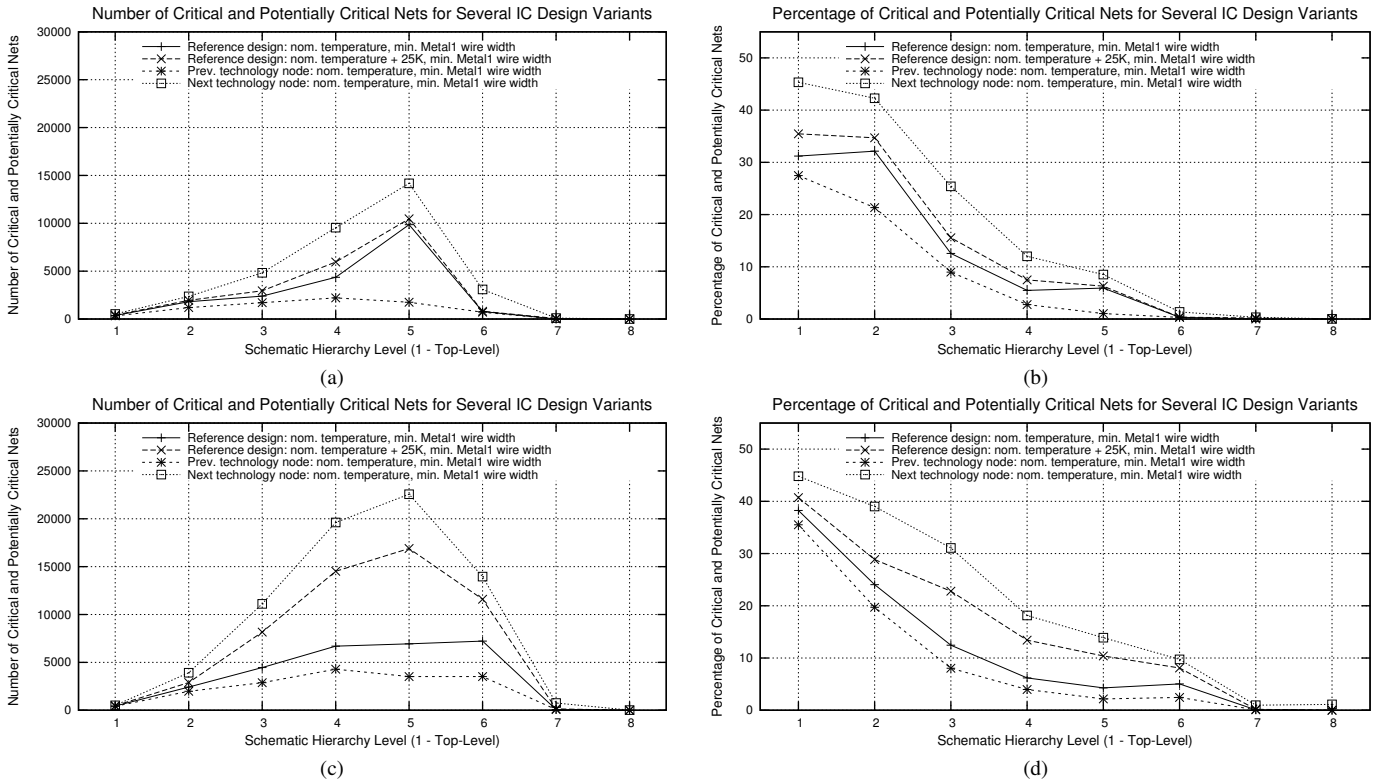

Fig. 6: Depiction of the number (6a, 6c) and percentage (6b, 6d) of current density critical nets throughout the schematic design hierarchy in IC design examples *Design1* (6a, 6b) and *Design2* (6c, 6d).

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