Methodology From Chaos in IC Implementation

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Abstract—Algorithms and tools used for IC implementation do not show deterministic and predictable behaviors with input parameter changes. Due to suboptimality and inaccuracy of underlying heuristics and models in EDA tools, overdesign using tighter constraints does not always result in better final design quality. Moreover, negligibly small input parameter changes can result in substantially different design outcomes.

In this paper, we assess the nature of 'chaotic' behavior in IC implementation tools via experimental analyses, and we determine a methodology to exploit such behavior based on the 'multi-run' and 'multi-start' sampling concepts proposed in [2]. We also suggest the number of sampling trials that yields more predictably good solutions; this allows us to improve quality of design without any manual analysis or manipulation, without changing any existing tool flows, and without unnecessary expenditure of valuable computing resources.

I. INTRODUCTION

With the rapid scaling of design complexity and quality requirements for system-on-chip products, electronic design automation (EDA) tools are confronted with ever-increasing problem difficulty and instance size. Virtually all underlying problem formulations within the IC implementation flow are NP-hard, and only heuristics - typically with unknown suboptimality - are usable in practice. In addition, due to the shrinking scale and large variability of nanometer process technologies, the modeling and analysis of physical problems are often fraught with accuracy challenges.

Commercial EDA tools and methodologies are used in production design because they improve turnaround times and design productivity. However, due to the suboptimality of underlying heuristics and the inaccuracy of underlying models and analyses, designers typically expect to spend significant time and effort after the tool flow is completed, to analyze remaining problems and fix them manually. To trade off quality of results versus implementation time and effort, designers must be able to *predict* the output quality of heuristic tools and methodologies. Based on their predictions, designers may target different objectives (e.g., minimizing area rather than performance), or different values of objectives (e.g., higher clock frequency, or lower leakage power).

With the above in mind, "predictability" is one of the most important attributes of IC design automation algorithms, tools and methodologies [1]. However, EDA heuristic approaches do not always behave according to users' intentions. Yakowitz et al. [5] study random search in machine learning under noise, and Kushner [4] analyzes the effect of noise in machine learning as stochastic approximation. Hartoog [3] observes the existence of noise in a VLSI algorithm and proposes exploitation of the noise to produce various benchmark circuits. At the first Physical Design Symposium in 1997, Ward Vercruysse of Sun Microsystems referred to the back-end implementation flow as a "chaos machine". The implication is that a very small change in inputs could lead to a very large change in outputs. In 2001, Kahng and Mantik [2] examined 'inherent noise' in IC implementation tools, i.e., how equivalent inputs could lead to different outputs.

In the present work, we assess the nature of 'chaotic' behavior in IC implementation tools, with an aim to establishing a beneficial methodology from such chaos. To assess the chaotic behavior, we experimentally determine answers to four questions:

- How strongly correlated are post-synthesis netlist quality and post-routing design quality?
- How strongly correlated are design quality as evaluated by vendor place-and route tools and design quality as evaluated by signoff tools?
- What chaotic behavior is associated with input parameters of vendor synthesis tools?
- What chaotic behavior is associated with input parameters of vendor place-and-route tools?

Our experimental analyses confirm substantial "chaos" in vendor tools, e.g., worst timing slack can vary by up to hundreds of picoseconds, and area can vary by up to 16.4%, in a given (65nm) block implementation. Furthermore, there is little correlation between major design stages.

Based on our experimental results, we establish a methodology to exploit the unavoidable noise and chaos in backend optimization tools. Our methodology is based on 'multirun' and/or 'multi-start' execution of the design flow with small, intentional input parameter perturbations. This recalls the work of [2], which also proposed the exploitation of 'inherent tool noise' to achieve more predictable and stable tool outcomes. A key difference between [2] and our work is that the 'noise' sources in [2] - renaming cell instances, perturbing the design hierarchy, etc. - are not practically usable. On the other hand, our proposed 'chaos' levers, such as changing clock uncertainty by 1 picosecond, are trivially implemented and transparent to the design flow. With the increasing availability of multiple and parallel computing platforms - multiple workstations in server farms, multiprocessor workstations, multicore processors, and multithreaded cores - our multi-run approach can be deployed with negligible impact on the overall design cycle time.¹ We also provide a method to find which input parameters are most sensitive to the perturbation, and optimal number of runs to obtain reasonably good and predictable solutions.

The remainder of this paper is organized as follows. In Section II, we examine our four motivational questions regarding the unpredictability and 'chaotic' nature of commercial tools.

¹In fact, since better-quality block implementations typically close faster, our approach can potentially reduce overall design cycle time.

We describe our proposed method for exploiting chaotic tool behavior in Section III. Finally, Section IV gives conclusions.

II. CHAOS IN IMPLEMENTATION TOOLS DUE TO INTENTIONAL INPUT DISTURBANCE

There are two basic types of knobs that affect the quality of optimization.

- **Tool-specific options** specifically, command options to turn on/off specific optimization heuristics. (We do not explore this, but use the same default tool options in all of our experiments.)
- **Design-specific constraints** notably timing-related constraints (clock cycle time, clock uncertainty, input/output minimum/maximum delay, etc.) and floorplan-related constraints (utilization, aspect ratio, primary pin locations, etc.).

In our study, we only examine the impact of intentional perturbation of design-specific constraints. For synthesis, we explore impact of timing-related constraints, and for placement and routing (P&R), we explore the impact of both timing- and floorplan-related constraints. We vary design-specific parameters by small amounts, and measure design quality metrics such as worst negative slack (WNS), total negative slack (TNS), and total standard-cell area.

We implement four testcases using a *TSMC* 65nm *GPLUS* library: two open-source cores, *AES* and *JPEG*, obtained as RTL from *opencores.org* [6], and two subblocks *LSU* (load and store unit) and *EXU* (execution unit) of the *OpenSparcT* 1 design, obtained from the *Sun OpenSPARC Projects* site [7]. We use a traditional timing-driven synthesis, placement and routing flow, and analyze final timing quality using a signoff RC extraction (*Synopsys STAR-RCXT* [13]) and a signoff static timing analyzer (*Synopsys PrimeTime* [10]). All specific tool versions are given in the references section below. Table I shows one of the implementation results for each of our testcases at the signoff stage. The remainder of this section describes our experimental investigation of the four motivating questions above - on the correlation between design stages, and on the chaotic behavior of implementation tools.

TABLE I

TESTCASE INFORMATION AT SIGNOFF WITH NOMINAL PARAMETER VALUES. IMPLEMENTATION USES *Synopsys Design Compiler* AND *Synopsys Astro.* 'SKEW' IS THE CLOCK UNCERTAINTY CONSTRAINT GIVEN AT SYNTHESIS STAGE TO ACCOUNT FOR CLOCK SKEW OCCURRING AT

PLACEMENT AND ROUTING STAGES.

Design	Cycle	Skew	IO	WNS	TNS	#Cells	Area
-	time	(<i>ns</i>)	Delay	(<i>ns</i>)	(<i>ns</i>)		(μm^2)
	(<i>ns</i>)		(<i>ns</i>)				
AES	1.7	0	0	-0.095	-0.210	22438	48957
JPEG	2.2	0	0	-0.224	-10.937	69845	178696
LSU	1.2	0	0	-0.327	-170.835	24945	113479
EXU	1.2	0	0	-0.760	-423.869	20382	69780

A. Correlation of Quality between Design Stages

Motivating Question 1: How strongly correlated are postsynthesis netlist quality and post-routing design quality?

It is by no means certain that a better-quality synthesized netlist will eventually lead to a better-quality design after placement and routing (P&R). Our first experiments examine the impact of the quality of input netlists on final P&R outcomes. We synthesize the *AES* core with various clock cycle times to have different timing quality at a target clock cycle time in synthesis. For each synthesized netlist, we perform placement and routing at the given target clock cycle time. We use *Cadence RTL Compiler* for synthesis and *Cadence SOC Encounter* for P&R.

Table II summarizes the worst negative slack values after synthesis and after P&R, respectively. The first column shows the clock cycle time applied at synthesis stage, and the second column shows the worst negative slack (WNS) with the target clock cycle time, i.e., 2ns. The third and fourth columns show the WNS values after placement and routing, obtained from Cadence SOC Encounter (SOCE) [9] and Synopsys PrimeTime (PT) [10], respectively.

TABLE II

TIMING QUALITY OF SYNTHESIZED NETLISTS VERSUS TIMING QUALITY AFTER PLACEMENT AND ROUTING, AND SIGNOFF.

Clock	WNS (ns)	Clock	WNS (ns)	WNS (ns)
used	with 2.0ns	used	from	from
synthesis	clock after	P&R	SOCE	PT
(ns)	synthesis	(ns)		
1.60	0.400	2.0	0.171	-0.249
1.80	0.200	2.0	0.088	-0.196
1.90	0.101	2.0	0.112	-0.195
1.95	0.051	2.0	0.074	-0.449
2.00	0.001	2.0	0.088	-0.252
2.10	-0.097	2.0	0.088	-0.214
2.20	-0.196	2.0	0.120	-0.281
2.40	-0.395	2.0	0.162	-0.081

From the data, we observe that an input netlist with better timing slack netlist does not always result in better timing slack after placement and routing. Furthermore, due to the timing miscorrelation between P&R and signoff tools, the worst-slack netlist from synthesis stage, obtained using largest clock cycle time (i.e., 2.4ns), actually results in the best timing at signoff. How this can occur is suggested by Figure 1, which gives a rank-correlation plot of endpoint slack values of timing paths in the *AES* netlist, between post-synthesis and postplacement stages. The correlation coefficient is only 0.421. Due to this miscorrelation between synthesis and P&R stages, the eventual benefit from maximizing the quality of the postsynthesis netlist is unclear. This gives us some intuition that any incremental tool runs should be directed to the P&R stage rather than the synthesis stage.



Fig. 1. Rank correlation of timing slack at all endpoints, i.e., input pins of all registers, between post-synthesis and post-placement stages for the *AES* designs.

Motivating Question 2: How strongly correlated are design quality as evaluated by vendor place-and route tools and design quality as evaluated by signoff tools?

Aside from the suboptimal nature of underlying optimization algorithms, there is another source of noise in the traditional implementation flow. Timing optimization is always based on (incremental) timing analysis. As is well known, such timing analysis requires models for gates and interconnect: timing and power models for gates are precharacterized in lookup tables using SPICE, and interconnect RC models are extracted from layout with precharacterized capacitance tables. Using the gate and interconnect models, effective load capacitance, slew degradation, interconnect delay are calculated using, e.g., asymptotic waveform estimation. The effective load capacitance and slew values thus obtained are then used as table indices to find corresponding gate delay values from delay tables. However, optimization tools use simplified models and embedded calculators to evaluate timing with the least possible computational expense. As a result, timing results seen by optimization tools can differ from those seen by signoff timing analysis tools.



Fig. 2. Worst negative slack correlation between a signoff timing analysis tool *Synopsys PrimeTime* on the y-axis, and implementation tools *Synopsys ASTRO* (rectangles) and *Cadence SOC Encounter* (diamonds) on the x-axis.

Figure 2 shows the timing correlation between a signoff timing analyzer *Synopsys PrimeTime*, equipped with a signoff RC extractor *Synopsys Star-RCXT*, and two place-and-route tools, *Synopsys Astro (ASTRO)* [11] and *Cadence SOC Encounter* (*SOCE*) [9], for 29 different implementations of the *AES* core. We observe that more than 200*ps* of timing slack difference can occur.

To understand methodology implications of P&R vs. signoff discrepancies, we make a brief excursion into root causes of such discrepancies. Typical root causes are as follows.

• **RC-extraction.** We extract RC values from a signoff extractor *Synopsys Star-RCXT (STAR)* and a place-and-route tool *Cadence SOC Encounter (SOCE)*. We compare the extracted capacitance values using the *Cadence Ostrich* program. Figure 3 compares the extracted capacitances from *STAR* with those from *SOCE*. We observe that *SOCE* underestimates capacitance by 18.6%.² This significant difference may explain why SOCE so consis-

tently sees optimistic timing slacks when compared to the signoff tool (Figure 2).



Fig. 3. Normalized capacitance correlation between a signoff RC extractor *Synopsys Star-RCXT (STAR)* on the x-axis, and a place-and-route tool Cadence SOC Encounter (*SOCE*) on the y-axis.

• **Delay calculation.** We compare timing between *SOCE* and *PT* with the same RC parasitic file from *SOCE*, to eliminate the impact of the discrepancy in RC extraction. Table IV shows the WNS and TNS calculated from both tools for our four testcases with default input parameters. The data suggests that delay calculation in *SOCE* and *PT* is well-correlated, as is usually the case. (N.B.: Viable implementation and signoff tools will calculate delay on a given extracted path to within at most a couple of tens of picoseconds difference from the 'golden' tool.)

TABLE III

WNS AND TNS FROM SIGNOFF TIMING ANALYZER Synopsys PrimeTime (PT) AND P&R TOOL Cadence SOC Encounter (SOCE), USING THE SAME RC PARASITICS FROM SOCE.

Design	P	Т	SO	CE			
•	WNS (ns)	TNS (ns)	WNS (ns)	TNS (ns)			
AES	0.144	0	0.146	0			
JPEG	0.129	0	0.095	0			
LSU	-0.002	-0.004	-0.005	-0.040			
EXU	-0.171	-11.483	-0.183	-12.669			

Other: Path-tracing and signal integrity in timing (1) Endpoint slack differences greater than analysis. several hundred picoseconds are typically due to discrepancies in path-tracing - i.e., the interpretation of timing constraints, timing exceptions, generated clocks, cyclebreaking in the timing graph, etc. - in the static timer. However, the testcases we use have only simple timing constraints consisting of one clock definition along with input/output delay constraints. Thus, path-tracing is not a factor in the timing miscorrelation between P&R and signoff in our experiments. (2) Endpoint slack differences on the order of 100ps are often due to discrepancies in signal integrity (e.g., crosstalk-induced delay variation) analyses. However, all timing analyses in our experiments are performed with signal integrity options turned off. Thus, signal integrity is not a factor in observed timing miscorrelations, either.

Although there is a discrepancy between place-and-route tools and signoff tools, we believe that this discrepancy (in all experimental data we report here) is systematic and attributable to internal RC extraction and path delay calculation. As shown in Figure 2, *SOCE* consistently underestimates the

 $^{^{2}}$ These data do not speak to the accuracy of extraction within a placeand-route tool. E.g., such a discrepancy may arise from a simplified twodimensional capacitance table given to the place-and-route tool.

timing slack. This correlated discrepancy can be predicted and compensated. We may infer that design quality at the P&R stage is a stronger lever on final signoff timing than design quality at the synthesis stage.

B. Chaotic Behavior in Optimization Tools

In this subsection, we assess the impact of intentional perturbations applied to input parameters of synthesis and place-and-route tools. (As noted above, the perturbations that we study differ from the netlist manipulations studied in [2], and are transparently applied without changing the design flow.)

Motivating Question 3: What chaotic behavior is associated with input parameters of vendor synthesis tools?

We analyze the impact of perturbation of timing-related parameters, such as clock cycle time, input/output delay, and clock uncertainty, at the synthesis stage. We use two commercial gate-level synthesis tools, *Synopsys Design Compiler* (*DC*) [12] and *Cadence RTL Compiler* (*RC*) [8]. We vary each parameter by an amount ranging from -3ps to 3ps with 1ps increments, and measure the changes in netlist quality metrics. Table II-B summarizes WNS and total standard-cell area of the resulting synthesized netlists.

Ideally, small perturbations of, e.g., a few picoseconds in input parameters should not change output quality, or should have predictable consequences. For example, a reduction of clock cycle time by 1 picosecond can be reasonably expected to result in a reduction of timing slack by the same 1 picosecond, since the difficulty of design optimization is virtually unchanged. However, due to the unpredictability of optimization tools, the resulting design quality appears to be random. We observe up to 53ps and 34ps of WNS variations in DC and in RC, respectively. Among the results, we observe that some input perturbations result in better timing quality than the original (without perturbations) design optimization. This improvement can be regarded as a benefit from 'chaotic behavior' of the design optimization tools. However, as discussed in Section II-A, input parameter perturbations at synthesis may not have a great effect on final signoff design quality, due to the unpredictable miscorrelation between synthesis and placeand-route tools.

Motivating Question 4: What chaotic behavior is associated with input parameters of vendor place-and-route tools?

We also analyze the impact of perturbations of both timingrelated parameters and floorplan-related parameters, in placeand-route tools. Since our second experiment above suggested that the quality of an input netlist is not preserved during placement and routing, we take one synthesized netlist arbitrarily from the synthesis results in the Table IV results, and perform traditional timing-driven placement and routing. We use two place-and-route tools, *Synopsys Astro (ASTRO)* and *Cadence SOC Encounter (SOCE)*. The nominal clock cycle time, input/output delay, and clock uncertainty values are shown in Table I, and nominal utilization and aspect ratio are 70% and 1.0, respectively.

Table V summarizes worst negative slack (WNS) and total negative slack (TNS) calculated using a signoff RC extraction and static timing analysis. We do not include the final area of placed and routed designs due to space limitations in the

table, but the variation of area is observed to be as high as 16.4% in the *AES* core when utilization is increased by just $1\%.^3$

From the table, we again observe that small input parameter perturbations give rise to large timing slack changes, e.g., WNS varies by up to 190ps (from -96ps to -287ps) in *EXU*, and TNS varies by more than 69ns (from -152ns to -83ns) in *JPEG*.

C. Summary of observations

Our experimental study provides the following evidence for 'chaotic behavior'.

- Input parameter perturbation in synthesis results in up to 53*ps* of WNS variation, and sometimes produces better-quality netlists than the original design constraints. However, because there is little correlation between post-synthesis netlist quality and post-routing design quality, improved synthesis results will not necessarily improve results after placement and routing.
- There is a large discrepancy in timing slack between optimization tools and signoff tools, which in our studies arises mainly from (i) the difference between optimization-internal and signoff RC extractors, and (ii) small discrepancies in delay calculation between optimization and signoff tools. Timing slack with the same RC parasitics can vary up to 34*ps* solely due to delay calculation discrepancies. However, the discrepancy may be predictable and hence compensatable.
- Input parameter perturbation in place-and-route tools results in up to 190*ps* of WNS variation, up to 46*ns* of TNS variation, and up to 16.4% variation in total standard-cell area. In contrast to chaos in synthesis outcomes, the chaos in place-and-route outcomes appears more exploitable to improve final signoff quality.
- This chaotic behavior is unpredictable. In particular, for different design types or domains, it may not be possible to assess differences in nature of the chaotic behavior. However, from Table V, we can observe that more timing-critical designs (e.g., designs with more negative timing slack, more violating paths, or smaller clock cycle time) tend to show more sensitivity to the input parameter perturbation.

III. PREDICTABILITY FROM CHAOS

In the previous section, we observed 'chaos': large variation in final implementation quality arising from small (negligible) input parameter changes. Frequently, results after small input perturbations are better than those obtained using nominal input parameter values. From the results, we expect that we can achieve better design quality (and, potentially, improved design cycle time) without additional human effort or flow modifications. The key idea: run multiple times with small input perturbations, and return the best-quality solution.

If only one CPU or tool license is available, then we can run multiple times on one CPU (*'multi-run'*), trading design quality for runtime. But when there are idle CPUs and licenses

³Because area and power are correlated, as the area changes, the design power is also affected by the input parameter perturbation. However, the degree of "chaos" for power will be less: WNS is a "max" attribute of the design, while power (as well as TNS) is a "sum" or "average" attribute.

TABLE IV

IMPACT OF INTENTIONAL PERTURBATIONS OF INPUT PARAMETERS FOR SYNTHESIS TOOLS. *RC* AND *DC* INDICATE RESULTS FROM *Cadence RTL Compiler* AND *Synopsys Design Compiler*, RESPECTIVELY. **BOLD** ENTRIES INDICATE MIN/MAX IN EACH EXPERIMENT.

Parameter	Noise (A)		A	ES		JPEG				
1 arameter	Noise (A)	1)C		RC	1)C		RC	
		WNS (ns)	Area (μm^2)	WNS (ns)	Area (μm^2)	WNS (ns)	Area (μm^2)	WNS (ns)	Area (μm^2)	
	-3ps	-0.243	42261	-0.051	50947	-0.154	300731	-0.120	220030	
	-2ps	-0.222	43986	-0.050	51036	-0.159	294333	-0.117	223779	
	-1ps	-0.218	44058	-0.047	50752	-0.169	299315	-0.122	220312	
Clock	0ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.110	224222	
Cvcle	lps	-0.229	42985	-0.048	50216	-0.177	298607	-0.118	219223	
	2ps	-0.232	42645	-0.041	51154	-0.174	298420	-0.112	216779	
	3ps	-0.216	44168	-0.041	51033	-0.148	299912	-0.110	222282	
	-3ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.111	223544	
	-2ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.110	222552	
	-1ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.109	223065	
Clock	0ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.110	224222	
Uncertainty	1ps	-0.227	43286	-0.046	50673	-0.165	299270	-0.108	223945	
-	2ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.107	222697	
	3ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.112	221580	
	-3ps	-0.216	44168	-0.041	51033	-0.174	298123	-0.110	222282	
	-2ps	-0.252	41892	-0.041	51154	-0.155	299840	-0.116	216878	
	-1ps	-0.234	42482	-0.048	50216	-0.177	298607	-0.118	219360	
IO Delay	0ps	-0.245	41735	-0.046	50673	-0.165	299270	-0.110	224222	
-	1ps	-0.233	42860	-0.047	50752	-0.164	299244	-0.121	220106	
	2ps	-0.222	43986	-0.050	51036	-0.164	299725	-0.115	223658	
	3ps	-0.216	44314	-0.051	50947	-0.169	299461	-0.123	221147	
Best	-	-0.216	-	-0.041	-	-0.148	-	-0.107	-	
Worst	-	-0.252	-	-0.051	-	-0.177	-	-0.123	-	
Delta	-	0.036	-	0.010	-	0.029	-	0.016	-	
					1					
Parameter	Noise (Δ)		LS	SU			EZ	YU	-	
Parameter	Noise (Δ)			SU I	RC	1	E2 DC	KU 1	१C	
Parameter	Noise (Δ)	WNS (ns)	$\frac{LS}{DC}$ Area (μm^2)	SU WNS (ns)	RC Area (μm^2)	WNS (ns)	$\frac{E\lambda}{DC}$ Area (μm^2)	XU WNS (ns)	RC Area (µm ²)	
Parameter	Noise (Δ) -3ps	UNS (ns) -0.110	LS DC Area (µm ²) 84943	SU WNS (ns) -0.042	<i>RC</i> Area (μm ²) 94275	UNS (ns) -0.133	<i>E2</i> <i>DC</i> Area (μm ²) 50685	<i>KU</i> WNS (<i>ns</i>) -0.040	<i>C</i> Area (μm ²) 58481	
Parameter	Noise (Δ) -3ps -2ps	UNS (ns) -0.110 -0.110	<i>LS</i> <i>DC</i> Area (<i>µm</i> ²) 84943 84983	SU WNS (ns) -0.042 -0.047	<i>RC</i> Area (μm ²) 94275 93995	UNS (ns) -0.133 -0.095		<i>KU</i> WNS (<i>ns</i>) -0.040 -0.052	RC Area (µm ²) 58481 58315	
Parameter	Noise (Δ) -3ps -2ps -1ps	UNS (ns) -0.110 -0.110 -0.102	<i>LS</i> <i>OC</i> Area (µm ²) 84943 84983 85166	SU WNS (<i>ns</i>) -0.042 -0.047 -0.042	<i>RC</i> Area (<i>µm</i> ²) 94275 93995 94450	U WNS (<i>ns</i>) -0.133 -0.095 -0.098	<i>E2</i> <i>DC</i> Area (µm ²) 50685 51661 51571	<i>KU</i> WNS (<i>ns</i>) -0.040 -0.052 -0.049	<i>RC</i> Area (µm ²) 58481 58315 58215	
Parameter	Noise (Δ) -3ps -2ps -1ps 0ps	UNS (ns) -0.110 -0.110 -0.102 -0.104	<i>LS</i> <i>OC</i> 84943 84983 85166 85052	<i>SU</i> WNS (<i>ns</i>) -0.042 -0.047 -0.042 -0.044	<i>C</i> <i>Area (µm²)</i> <i>94275</i> <i>93995</i> <i>94450</i> <i>94119</i>	UNS (ns) -0.133 -0.095 -0.098 -0.128	<i>E2</i> <i>OC</i> 50685 51661 51571 50442	<i>KU</i> WNS (<i>ns</i>) -0.040 -0.052 -0.049 -0.042	<i>RC</i> Area (µm ²) 58481 58315 58215 58287	
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps	UNS (ns) -0.110 -0.102 -0.104 -0.105	LS DC Area (µm ²) 84943 84983 85166 85052 84747	SU WNS (<i>ns</i>) -0.042 -0.047 -0.042 -0.044 -0.046	<i>C</i> Area (μm ²) 94275 93995 94450 94119 93509	Z WNS (<i>ns</i>) -0.133 -0.095 -0.098 -0.128 -0.108	<i>E2</i> <i>DC</i> 50685 51661 51571 50442 50858	XU WNS (<i>ns</i>) -0.040 -0.052 -0.049 -0.042 -0.057	<i>RC</i> Area (µm ²) 58481 58315 58215 58287 58330	
Parameter	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps	UNS (ns) -0.110 -0.102 -0.104 -0.105 -0.101 -0.105	LS DC Area (µm ²) 84943 84983 85166 85052 84747 84915 84915	SU -0.042 -0.047 -0.044 -0.044 -0.046 -0.044 -0.044	RC Area (μm ²) 94275 93995 94450 94119 93509 92629 92629	UNS (ns) -0.133 -0.095 -0.098 -0.128 -0.108 -0.145 -0.145	<i>E2</i> <i>OC</i> 50685 51661 51571 50442 50858 50314	XU WNS (<i>ns</i>) -0.040 -0.052 -0.049 -0.042 -0.042 -0.057 -0.036	RC Area (µm ²) 58481 58315 58215 58287 58330 58217 58330	
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps	UNS (ns) -0.110 -0.102 -0.104 -0.105 -0.101 -0.108	LS DC Area (μm ²) 84943 84983 85166 85052 84747 84915 84904	SU WNS (<i>ns</i>) -0.042 -0.047 -0.044 -0.044 -0.046 -0.044 -0.046	RC Area (μm ²) 94275 93995 94450 94119 93509 92629 92028 92028	UNS (ns) -0.133 -0.095 -0.098 -0.128 -0.108 -0.145 -0.099	<i>E2</i> <i>OC</i> Area (μm ²) 50685 51661 51571 50442 50858 50314 51221 51221	XU WNS (ns) -0.040 -0.052 -0.049 -0.042 -0.057 -0.036 -0.032	<i>RC</i> Area (µm ²) 58481 58315 58215 58287 58330 58217 58044	
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps	<u>U</u> WNS (<i>ns</i>) -0.110 -0.102 -0.104 -0.105 -0.101 -0.108 -0.104	LS DC Area (µm ²) 84943 84983 85166 85052 84747 84915 84904 85086 85086	SU -0.042 -0.047 -0.042 -0.044 -0.044 -0.046 -0.044 -0.046 -0.046 -0.048	<i>RC</i> 94275 93995 94450 94119 93509 92629 92028 93000 93000	UNS (ns) -0.133 -0.095 -0.098 -0.128 -0.108 -0.145 -0.099 -0.115	E2 CC 50685 51661 51571 50442 50858 50314 51221 50763 50763	XU WNS (ns) -0.040 -0.052 -0.049 -0.042 -0.042 -0.036 -0.036 -0.032 -0.026	<i>RC</i> 58481 58315 58215 58287 58330 58217 58044 58264	
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 3ps -3ps -2ps	UNS (ns) -0.110 -0.110 -0.102 -0.104 -0.105 -0.101 -0.108 -0.104 -0.108	LS OC Area (µm²) 84943 84983 85166 85052 84747 84915 84994 85086 84928 84928	SU -0.042 -0.047 -0.042 -0.044 -0.044 -0.046 -0.048 -0.045 -0.045	<i>RC</i> 94275 93995 94450 94119 93509 92629 92028 93000 93594 93594	UNS (ns) -0.133 -0.005 -0.098 -0.128 -0.108 -0.145 -0.099 -0.115 -0.124 -0.124	<i>E2</i> <i>OC</i> 50685 51661 51571 50442 50858 50314 51221 50763 50638	XU WNS (ns) -0.040 -0.052 -0.049 -0.042 -0.057 -0.036 -0.032 -0.026 -0.046	<i>RC</i> 58481 58315 58215 58287 58330 58217 58044 58264 58264 58463	
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Parameter Clock Cycle Clock Uncertainty IO Delay Best Worst Delta	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -1ps 0ps 1ps 2ps 3ps -1ps 0ps 1ps 2ps 3ps - -	Z WNS (ns) -0.110 -0.102 -0.104 -0.105 -0.108 -0.108 -0.104 -0.105 -0.101 -0.108 -0.104 -0.105 -0.104 -0.105 -0.104 -0.105 -0.104 -0.105 -0.104 -0.105 -0.106 -0.107 -0.107 -0.100 -0.101 -0.102 -0.103 -0.104 -0.107 -0.110 -0.112 -0.011	LS DC Area (µm ²) 84943 84983 85166 85052 84747 84915 84904 85086 84928 85007 85052 84840 84744 85097 84834 84757 84834 84757 84639 85052 84863 85101 84833 - -	SU WNS (ns) -0.042 -0.047 -0.044 -0.044 -0.046 -0.044 -0.046 -0.044 -0.046 -0.048 -0.048 -0.045 -0.048 -0.045 -0.044 -0.045 -0.044 -0.045 -0.042 -0.045 -0.044 -0.045 -0.054 -0.055	RC 94275 93995 94450 94119 93509 92629 92028 93000 93594 94350 94119 93983 93729 93743 92105 93817 94372 94119 94218 944128 94010 -	L WNS (ns) -0.133 -0.095 -0.098 -0.128 -0.108 -0.145 -0.099 -0.115 -0.124 -0.127 -0.128 -0.117 -0.128 -0.117 -0.125 -0.125 -0.125 -0.128 -0.098 -0.095 -0.147	E2 CC SO(85) 50685 51661 51571 50442 50858 50314 51221 50763 50638 49995 50442 50575 50804 50329 51221 50995 50483 50483 50483 50484 51571 51661 51661 50685 - -	XU I WNS (ns) -0.040 -0.052 -0.049 -0.032 -0.036 -0.032 -0.026 -0.044 -0.031 -0.026 -0.046 -0.031 -0.046 -0.029 -0.046 -0.049 -0.042 -0.042 -0.035 -0.042 -0.042 -0.042 -0.042 -0.042 -0.042 -0.042 -0.042 -0.042 -0.040 -0.042 -0.040 -0.042 -0.049 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.040 -0.057 -0.034	RC Area (µm ²) 58481 58315 58215 58287 58330 58217 58044 58463 58508 58287 58453 58543 58543 58543 58543 58543 58217 58434 58217 58217 58434 58215 58227 58217 58434 58287 58217 58434 58287 58217 58434 58287 58218 58543 58543 58543 58217 58217 58481 58543 58217 58434 58543 58544 58545 58544 58545 58555 585555 5855555 585555555555	

in a large computing farm, we may be able to use as many CPUs as possible in parallel (*'multi-start'*) without affecting the design cycle time. In either scenario, we obtain a "best-of-k" methodology: (i) run k times on a CPU while varying input parameter values, or (ii) start k runs with different input parameter values, and take the best results out of the k different runs.

If we wish to experimentally determine the best number k of runs - in a statistically meaningful manner - it at first seems necessary to execute many trials for each possible value of k. For example, we could conduct N trials each with a set of k runs, then record the best solution out of each set of k runs, and then find the average ('expected') best solution for the given value of k. If we know the average best-of-k solution value for each value of k, then we can determine which k gives reasonably good solutions compared to the cost of resources. The challenge is that the above-described procedure requires far too many runs. Naively, if we run N trials of "best-of-k" runs, we may require $N \times k$ separate runs. And if we test six

different values of k numbers - e.g., 1, 2, 3, 4, 5, and 10 - through 100 trials, we would have to perform $100 \times (1 + 2 + 3 + 4 + 5 + 10) = 2500$ separate runs.

To reduce the number of test runs needed to determine the best k value, we use the following sampling approach, which was originally presented in [2].

- 1) Run a smaller number of different runs, e.g., 50 times with different inputs, instead of 2500 runs as in the previous example.
- 2) Record a quality metric, e.g., WNS, for each run. Then, assume that the set of solutions for the 50 runs is the 'virtual' solution space.
- Randomly sample k solutions out of the 'virtual' solution space N=100 times, and record the best results for each choice of k solutions. This process replaces the actual N trials of k runs each.
- 4) Find minimum, maximum, and average values of the best results recorded from the *N* sampling trials.
- For our experiments, we use this "best-of-k" method out of

TABLE V

IMPACT OF INTENTIONAL PERTURBATION OF INPUT PARAMETERS IN PLACEMENT AND ROUTING TOOLS. *ASTRO* AND *SOCE* REPRESENT THE RESULTS FROM *Synopsys Astro* AND *Cadence SOC Encounter*, RESPECTIVELY. **BOLD** ENTRIES INDICATE MIN/MAX IN EACH EXPERIMENT.

Parameter	Noise (Δ)		Al	ES	S JPEG			EG	
		AST	RO	SOC	CE	AST	TNS (mc)	SO WNS (mg)	CE
	-3ps	-0.105	-1.388	-0.039	-0.183	-0.170	-40.785	-0.188	-127.129
	-2ps	-0.105	-1.398	-0.033	-0.117	-0.160	-29.732	-0.205	-91.147
~	-1ps	-0.097	-1.135	-0.035	-0.189	-0.183	-28.936	-0.186	-147.223
Clock	0ps	-0.102	-1.109	-0.084	-0.287	-0.234	-58.009	-0.198	-140.570
Cycle	2ns	-0.107	-1.511	-0.058	-0.435	-0.209	-42.422	-0.193	-138 579
	3ps	-0.106	-1.503	-0.053	-0.220	-0.196	-34.022	-0.183	-135.538
	-3ps	-0.107	-1.500	-0.084	-0.287	-0.136	-32.186	-0.192	-119.593
	-2ps	-0.107	-1.500	-0.084	-0.287	-0.204	-34.042	-0.191	-104.662
Clock	-1ps Ops	-0.107	-1.500	-0.084	-0.287	-0.187	-52.320	-0.208	-129.670
Uncertainty	1ps	-0.112	-1.119	-0.084	-0.287	-0.172	-32.838	-0.177	-99.811
	2ps	-0.114	-1.119	-0.084	-0.287	-0.141	-28.878	-0.188	-140.688
	3ps	-0.114	-1.119	-0.084	-0.287	-0.157	-25.764	-0.197	-103.762
	-3ps	-0.106	-1.503	-0.053	-0.220	-0.159	-29.123	-0.183	-135.538
	-2ps	-0.106 -0.107	-1.511	-0.058	-0.435	-0.227	-54.296	-0.180	-138.579
IO	0ps	-0.107	-1.109	-0.084	-0.287	-0.234	-58.009	-0.195	-140.570
Delay	1ps	-0.097	-1.135	-0.035	-0.189	-0.249	-65.507	-0.186	-147.223
	2ps	-0.105	-1.398	-0.033	-0.117	-0.157	-31.410	-0.205	-91.147
	3ps	-0.105	-1.388	-0.039	-0.183	-0.198	-42.760	-0.188	-127.129
	-0.03	-0.104	-1.480	-0.036	-0.214	-0.132	-20.743	-0.200	-152.493
	-0.02	-0.114	-1.512	-0.030	-0.214	-0.185	-42.322	-0.183	-139 986
Aspect	0.00	-0.102	-1.109	-0.084	-0.287	-0.234	-58.009	-0.198	-140.570
Ratio	0.01	-0.112	-1.520	-0.041	-0.269	-0.145	-38.358	-0.195	-123.821
	0.02	-0.136	-1.974	-0.041	-0.269	-0.193	-44.742	-0.203	-120.917
	0.03	-0.120	-1.868	-0.061	-0.439	-0.166	-20.162	-0.222	-102.049
	-5%	-0.149	-3.106	-0.046	-0.339	-0.186	-42.323	-0.173	-82.535
	-1%	-0.127	-2.057	-0.002	-0.274	-0.209	-44.032	-0.187	-133.042
Placement	0%	-0.102	-1.109	-0.084	-0.287	-0.234	-58.009	-0.198	-140.570
Utilization	1%	-0.133	-1.235	-0.112	-5.392	-0.133	-27.029	-0.187	-107.559
	2%	-0.132	-2.126	-0.046	-0.543	-0.139	-24.120	-0.179	-96.438
Deet	3%	-0.129	-1.390	-0.046	-0.679	-0.140	-19.303	-0.190	-105.871
Worst	-	-0.097	-1.109	-0.033	-0.113	-0.132	-19.303	-0.1/3	-82.535
Delta	-	0.051	1.997	0.080	5.279	0.117	46.204	0.049	69.958
Parameter	Noise (A)		LS	SU			EZ	<u>YU</u>	
Parameter	Noise (Δ)	AST	LS TRO	SU SO	CE	AST	EX TRO	KU SO	CE
Parameter	Noise (Δ)	AST WNS (ns)	LS TRO TNS (ns)	SU SOC WNS (ns)	CE TNS (ns)	AST WNS (ns)	E2 TRO TNS (ns)	XU SO WNS (ns)	CE TNS (ns)
Parameter	Noise (Δ)	AST WNS (ns) -0.104	<i>LS</i> <i>TRO</i> TNS (<i>ns</i>) -2.061	SU SO WNS (<i>ns</i>) -0.146 0.164	CE TNS (<i>ns</i>) -26.218	AST WNS (ns) -0.307	E2 TRO TNS (ns) -1.945 2 472	<i>XU</i> <i>SO</i> WNS (<i>ns</i>) -0.174 0.161	CE TNS (<i>ns</i>) -2.828 2.040
Parameter	Noise (Δ) -3ps -2ps -1ps	AST WNS (ns) -0.104 -0.082 -0.142	<i>LS</i> <i>TRO</i> -2.061 -1.298 -3.539	SU SO WNS (<i>ns</i>) -0.146 -0.164 -0.171	CE TNS (ns) -26.218 -27.249 -27.489	AST WNS (ns) -0.307 -0.262 -0.271	E2 RO TNS (ns) -1.945 -2.472 -3.869	<i>XU</i> <i>SO</i> WNS (<i>ns</i>) -0.174 -0.161 -0.287	CE TNS (ns) -2.828 -2.940 -8.692
Parameter	Noise (Δ) -3ps -2ps -1ps 0ps	AST WNS (<i>ns</i>) -0.104 -0.082 -0.142 -0.127	<i>LS</i> <i>RO</i> <i>TNS (ns)</i> -2.061 -1.298 -3.539 -5.096	SU SO WNS (<i>ns</i>) -0.146 -0.164 -0.171 -0.140	CE -26.218 -27.249 -27.489 -21.140	AST WNS (<i>ns</i>) -0.262 -0.271 -0.160	<i>E2</i> <i>RO</i> -1.945 -2.472 -3.869 -2.740	<i>KU</i> WNS (<i>ns</i>) -0.174 -0.161 -0.287 -0.164	CE TNS (ns) -2.828 -2.940 -8.692 -3.314
Parameter Clock Cycle	-3ps -2ps -1ps 0ps 1ps	AS7 WNS (<i>ns</i>) -0.104 -0.082 -0.142 -0.127 -0.116	LS RO -2.061 -1.298 -3.539 -5.096 -1.735	SU SO(WNS (ns) -0.146 -0.164 -0.171 -0.140 -0.130	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237	<i>E2</i> <i>RO</i> -1.945 -2.472 -3.869 -2.740 -2.084	<i>KU</i> WNS (<i>ns</i>) -0.174 -0.161 -0.287 -0.164 -0.177	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps	AST WNS (<i>ns</i>) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144	LS RO -2.061 -1.298 -3.539 -5.096 -1.735 -3.611	SU SO WNS (<i>ns</i>) -0.146 -0.164 -0.171 -0.140 -0.130 -0.167	CE -26.218 -27.249 -27.489 -21.140 -20.008 -28.938	<i>AST</i> WNS (<i>ns</i>) -0.262 -0.271 -0.160 -0.237 -0.267	<i>E2</i> <i>RO</i> -1.945 -2.472 -3.869 -2.740 -2.084 -3.992	KU SO WNS (<i>ns</i>) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178	CE -2.828 -2.940 -8.692 -3.314 -2.403 -2.693
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps	AST WNS (<i>ns</i>) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090	<i>LS</i> <i>TNS (ns)</i> -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508	SU SO WNS (<i>ns</i>) -0.146 -0.164 -0.171 -0.140 -0.130 -0.167 -0.178	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584	AST WNS (ns) -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.274	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430	<i>KU</i> <i>SO</i> <i>-0.174</i> <i>-0.161</i> <i>-0.164</i> <i>-0.177</i> <i>-0.178</i> <i>-0.096</i>	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -1.191
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps	AS7 WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 0.507	SU SO WNS (<i>ns</i>) -0.146 -0.164 -0.171 -0.140 -0.167 -0.167 -0.167 -0.182 0.159	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.959	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.474	<i>KU</i> <i>SO</i> <i>WNS (ns)</i> -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.176 0.157	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 2.554
Parameter Clock Cycle	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps -3ps -2ps -1ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.108	Ls 'RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674	SOU SOU WNS (ns) -0.146 -0.158 -0.167 -0.167	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424	XU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.176 -0.157 -0.157 -0.133	CE TNS (ns) -2.828 -2.940 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086
Parameter Clock Cycle Clock	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps -2ps -3ps -2ps -3ps -2ps -1ps 0ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127	LS 'RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096	SOU WNS (ns) -0.146 -0.158 -0.167	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.267 -0.267 -0.262 -0.271 -0.160	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740	XU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.176 -0.157 -0.153 -0.164	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314
Parameter Clock Cycle Clock Uncertainty	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps -3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -1ps 0ps 1ps 1ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140	Ls 'RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462	SU 0.146 -0.164 -0.164 -0.167 -0.180 -0.181 -0.158 -0.158 -0.156	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.267 -0.267 -0.257 -0.160 -0.300	E2 RO TNS (ns) -1.945 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832	XU VNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.153 -0.164 -0.159	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -3.314 -2.354
Parameter Clock Cycle Clock Uncertainty	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps -1ps 0ps 1ps 2ps 2ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140 -0.127 -0.140 -0.127 -0.120 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.127 -0.125 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.120 -0.127 -0.120 -0.120 -0.127 -0.120	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -2.081	SOU SOU WNS (ns) -0.146 -0.140 -0.140 -0.140 -0.167 -0.159 -0.158 -0.156 -0.156 -0.156 -0.130	CE TNS (ns) -26,218 -27,249 -27,489 -21,140 -20,008 -28,938 -25,584 -27,546 -28,859 -21,579 -21,140 -24,432 -23,977 -21,140 -24,92 -23,977 -21,140 -24,92 -23,977 -21,140 -24,92 -24,92 -25,584 -27,546 -27,546 -28,938 -21,579 -21,140 -20,008 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,546 -27,97 -21,140 -20,008 -21,140 -20,008 -21,140 -21,140 -21,140 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -22,97 -21,140 -23,97 -23,977 -23,977 -23,977 -27,140 -24,977 -23,977 -27,140 -24,977 -27,140 -24,977 -27,140 -24,977 -27,140 -27,576 -27,576 -27,576 -27,576 -27,576 -27,576 -27,576 -27,576 -27,576 -27,577 -27,140 -27,577 -27,140 -27,577 -27,140 -27,577 -27,5	AST WNS (ns) -0.362 -0.262 -0.271 -0.267 -0.267 -0.267 -0.257 -0.160 -0.257 -0.160 -0.257 -0.160 -0.257 -0.160 -0.257 -0.160 -0.257 -0.160 -0.257 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.257 -0.267 -0.257 -0.257 -0.257 -0.257 -0.257 -0.257 -0.257 -0.257 -0.257 -0.257 -0.257 -0.257 -0.250	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -4.424 -3.832 -2.292 -2.740 -3.832 -2.292	SO WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.153 -0.164 -0.157 -0.163 -0.159 -0.163	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.817 -2.817
Parameter Clock Cycle Clock Uncertainty	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps 3ps 3ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.125 -0.140 -0.127 -0.140 -0.125 -0.142 -0.127 -0.140 -0.125 -0.142 -0.127 -0.153 -0.127 -0.153 -0.127 -0.153 -0.127 -0.153 -0.127 -0.153 -0.127 -0.153 -0.127 -0.153 -0.127 -0.153 -0.127 -0.153 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.153 -0.153 -0.113 -0.127 -0.140 -0.153 -0.127 -0.140 -0.153 -0.127 -0.140 -0.153 -0.127 -0.140 -0.153 -0.155	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114	SO SO WNS (ns) -0.146 -0.171 -0.140 -0.164 -0.171 -0.182 -0.159 -0.156 -0.130 -0.156 -0.137	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.228	AST WNS (ns) -0.362 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.267 -0.160 -0.257 -0.160 -0.230 -0.241 -0.241 -0.241	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.852 -2.292 -6.533 -6.64	SO WNS (ns) -0.174 -0.61 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.157 -0.164 -0.157 -0.163 -0.164 -0.157 -0.163 -0.164 -0.164 -0.168 -0.168	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -2.256 -1.191
Parameter Clock Cycle Clock Uncertainty	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -3ps -3ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.124 -0.125 -0.108 -0.209 -0.125 -0.108 -0.209 -0.127 -0.140 -0.120 -0.156	LS RO -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401	SO SO WNS (ns) -0.146 -0.171 -0.164 -0.171 -0.182 -0.159 -0.156 -0.130 -0.156 -0.156 -0.150 -0.156	CE -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.267 -0.267 -0.160 -0.257 -0.160 -0.300 -0.245 -0.245 -0.245	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769	SO WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.153 -0.164 -0.159 -0.163 -0.163 -0.163 -0.164	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693
Parameter Clock Cycle Clock Uncertainty	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps -3ps -3ps -3ps -3ps -3ps -3ps -2ps -3ps -3ps -3ps -2ps -1ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127 -0.110 -0.120 -0.120 -0.113 -0.113 -0.160 -0.136	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728	SU SO(0 WNS (ns) -0.146 -0.171 -0.130 -0.167 -0.178 -0.159 -0.158 -0.140 -0.158 -0.156 -0.150 -0.150	CE -26.218 -27.249 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.267 -0.267 -0.267 -0.267 -0.257 -0.160 -0.257 -0.160 -0.220 -0.245 -0.2277 -0.169	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905	SO WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.153 -0.163 -0.163 -0.163 -0.163 -0.163 -0.178 -0.178	CE -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.554 -2.817 -2.256 -1.191 -2.693 -2.403
Parameter Clock Cycle Clock Uncertainty	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -3ps -1ps 0ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.125 -0.108 -0.209 -0.125 -0.108 -0.209 -0.127 -0.140 -0.153 -0.140 -0.136 -0.127	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096	SU SOU WNS (ns) -0.146 -0.171 -0.130 -0.167 -0.158 -0.158 -0.156 -0.130 -0.156 -0.157	CE TNS (ns) -26.218 -27.249 -27.249 -27.489 -21.140 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140	AST WNS (ns) -0.307 -0.262 -0.271 -0.267 -0.267 -0.267 -0.267 -0.267 -0.257 -0.160 -0.200 -0.241 -0.245 -0.277 -0.169 -0.160	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.992 -6.533 -6.694 -4.769 -2.905 -2.740	SO WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.163 -0.164 -0.159 -0.168 -0.068 -0.177 -0.164	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.354 -2.354 -2.354 -2.354 -2.256 -1.191 -2.693 -2.403 -3.314
Parameter Clock Cycle Clock Uncertainty	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps 3ps -3ps -2ps 3ps -3ps -2ps -1ps 0ps 1ps -1ps 1ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.125 -0.125 -0.120 -0.121 -0.125 -0.125 -0.120 -0.120 -0.133 -0.160 -0.136 -0.127 -0.126	Ls 'RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -2.970	SOU SOU WNS (ns) -0.146 -0.171 -0.130 -0.164 -0.171 -0.140 -0.130 -0.167 -0.158 -0.159 -0.156 -0.150 -0.156 -0.156 -0.156 -0.156 -0.156 -0.150 -0.140 -0.141	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -25.409 -21.140 -25.409 -21.140 -25.409 -21.140 -25.409 -21.140 -25.409 -21.140 -25.409 -21.140 -25.409 -21.140 -25.409 -21.140 -25.409 -21.140 -25.208 -21.140 -25.208 -21.140 -25.208 -21.140 -25.208 -21.140 -25.208 -21.140 -25.208 -21.140	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.186 -0.257 -0.160 -0.200 -0.241 -0.245 -0.277 -0.169 -0.160 -0.173	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.929 -6.533 -6.694 -4.769 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -2.740 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.859 -2.740 -3.852 -2.740 -3.459 -2.740 -3.757 -2.740 -3.757 -2.740 -3.757 -2.740 -3.757 -2.740 -3.7	SO VU SO -0.174 -0.161 -0.287 -0.164 -0.177 -0.177 -0.178 -0.096 -0.157 -0.153 -0.164 -0.159 -0.163 -0.163 -0.178 -0.164 -0.178 -0.163	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.354 -2.817 -2.256 -1.191 -2.693 -2.693 -3.314 -8.692 -3.314 -8.692
Parameter Clock Cycle Clock Uncertainty IO Delay	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps -3ps -2ps -1ps 0ps 1ps 2ps -3ps -2ps -1ps 0ps 1ps 2ps -3ps -2ps -1ps 0ps -2ps -1ps 0ps 1ps 2ps -2ps -1ps 0ps 1ps 2ps 3ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140 -0.120 -0.153 -0.135 -0.145 -0.145 -0.155	Ls 'RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.177 -2.066 -2.970	SOU SOU WNS (ns) -0.146 -0.171 -0.130 -0.164 -0.171 -0.140 -0.130 -0.153 -0.159 -0.156 -0.150 -0.156 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150 -0.150	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -25.409 -18.943 -23.232	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.262 -0.271 -0.267 -0.260 -0.271 -0.260 -0.271 -0.260 -0.271 -0.260 -0.277 -0.260 -0.277 -0.269 -0.277 -0.269 -0.277 -0.269 -0.277 -0.169 -0.217 -0.169 -0.207 -0.173 -0.207 -0.173 -0.207 -0.207 -0.173 -0.207	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.929 -6.533 -6.694 -4.769 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -3.5755 -2.740 -3.5555 -2.7555	SO VU SO -0.174 -0.161 -0.287 -0.164 -0.177 -0.177 -0.178 -0.096 -0.157 -0.163 -0.164 -0.159 -0.168 -0.096 -0.177 -0.163 -0.168 -0.096 -0.177 -0.164	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -8.692 -2.940 2.970
Parameter Clock Cycle Clock Uncertainty IO Delay	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps 0ps 1ps 2ps 3ps 0ps 0ps 0ps 0ps 0ps 0ps 0ps 0ps 0ps 0ps	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140 -0.127 -0.140 -0.127 -0.113 -0.113 -0.114 -0.139	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.177 -2.006	SO SO WNS (ns) -0.146 -0.171 -0.140 -0.164 -0.171 -0.182 -0.159 -0.159 -0.156 -0.137 -0.156 -0.156 -0.150 -0.151 -0.150 -0.150 -0.151 -0.152 -0.152	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -6.238 -30.726 -48.136 -21.140 -25.409 -18.943 -23.232 -20.466	AST WNS (ns) -0.362 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.267 -0.160 -0.257 -0.160 -0.241 -0.245 -0.245 -0.277 -0.169 -0.160 -0.302	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -1.595 -3.425	SOU SOU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.176 -0.157 -0.163 -0.164 -0.176 -0.163 -0.164 -0.178 -0.168 -0.096 -0.178 -0.164 -0.287 -0.164 -0.174	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.693 -2.403 -2.828 -2.940 -2.828 -2.828 -2.940 -2.828 -2.940 -2.828 -2.940 -2.828 -2.940 -2.828 -2.940 -2.940 -2.828 -2.940 -2.828 -2.940
Parameter Clock Cycle Clock Uncertainty IO Delay	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.124 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.125 -0.125 -0.113 -0.125 -0.114 -0.125 -0.113 -0.125 -0.114 -0.127 -0.125 -0.127 -0.125 -0.125 -0.127 -0.125 -0.127 -0.125 -0.125 -0.127 -0.125 -0.127 -0.125 -0.125 -0.127 -0.125 -0.125 -0.127 -0.125 -0.127 -0.125 -0.125 -0.127 -0.127 -0.125 -0.125 -0.127 -0.127 -0.125 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.125 -0.136 -0.125 -0.136 -0.125 -0.136 -0.137 -0.136 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.139 -0.142 -0.142 -0.139 -0.142 -0.142 -0.139 -0.142 -0.142 -0.139 -0.142 -0.142 -0.142 -0.142 -0.139 -0.142 -0.142 -0.142 -0.139 -0.142 -0.142 -0.142 -0.142 -0.139 -0.142	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -1.771 -2.006 -1.771 -2.006	SU SO(WNS (ns) -0.164 -0.171 -0.182 -0.167 -0.178 -0.159 -0.156 -0.130 -0.156 -0.156 -0.150 -0.156 -0.156 -0.158 -0.150 -0.150	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -25.409 -18.943 -23.232 -20.466 -27.070	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274 -0.257 -0.160 -0.300 -0.245 -0.277 -0.169 -0.160 -0.173 -0.207 -0.302 -0.299 -0.220	E2 RO -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.852 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.852 -2.905 -2.740 -3.852 -2.905 -2.740 -3.852 -5.755 -1.595 -3.425 -6.548	SOU SOU WNS (ns) -0.174 -0.287 -0.164 -0.177 -0.178 -0.096 -0.163 -0.164 -0.157 -0.163 -0.164 -0.159 -0.163 -0.164 -0.177 -0.164 -0.177 -0.164 -0.177 -0.164 -0.174 -0.233 -0.174	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.693 -2.403 -2.817 -2.256 -1.191 -2.693 -2.403 -2.828 -2.940 -2.940
Parameter Clock Cycle Clock Uncertainty IO Delay	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.124 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140 -0.120 -0.123 -0.113 -0.160 -0.125 -0.113 -0.125 -0.114 -0.125 -0.113 -0.125 -0.114 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.125 -0.127 -0.127 -0.127 -0.125 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.140 -0.125 -0.125 -0.127 -0.140 -0.125 -0.125 -0.127 -0.140 -0.125 -0.125 -0.127 -0.140 -0.125 -0.114 -0.120 -0.125 -0.114 -0.120 -0.125 -0.114 -0.129 -0.142 -0.125 -0.114 -0.129 -0.142 -0.125 -0.114 -0.129 -0.142 -0.125 -0.114 -0.129 -0.142 -0.123 -0.142 -0.142 -0.230	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -1.771 -2.006 -1.721 -0.625 -3.382	SU SOU WNS (ns) -0.146 -0.171 -0.180 -0.167 -0.178 -0.182 -0.159 -0.156 -0.156 -0.156 -0.150 -0.156 -0.158 -0.158 -0.158 -0.158 -0.158 -0.158 -0.160 -0.160	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274 -0.267 -0.160 -0.300 -0.245 -0.277 -0.169 -0.169 -0.173 -0.207 -0.302 -0.299 -0.220 -0.152	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.852 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -1.595 -3.425 -6.548 -2.934	SOU SOU WNS (ns) -0.174 -0.287 -0.164 -0.177 -0.164 -0.178 -0.096 -0.153 -0.163 -0.163 -0.163 -0.164 -0.176 -0.163 -0.164 -0.159 -0.163 -0.164 -0.178 -0.174 -0.287 -0.161 -0.174 -0.233 -0.174	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.554 -2.086 -2.554 -2.086 -3.314 -2.554 -2.554 -2.086 -2.554 -2.086 -2.554 -2.086 -2.554 -2.086 -2.554 -2.086 -2.554 -2.093 -2.554 -2.093 -2.403 -2.569 -2.593 -2.940 -2.590 -2.940 -2.590 -2.940 -2.507 -2.940 -2.507 -2.940 -2.507 -3.314 -3.314 -3.314 -3.314 -3.314 -3.306 -5.307
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -00s -0.03 -0.02 -0.01 0.00	AST WNS (ns) -0.108 -0.142 -0.127 -0.116 -0.125 -0.108 -0.125 -0.140 -0.123 -0.124 -0.125 -0.108 -0.120 -0.121 -0.136 -0.136 -0.125 -0.136 -0.125 -0.136 -0.125 -0.136 -0.125 -0.136 -0.125 -0.136 -0.125 -0.136 -0.1230 -0.1230	Ls RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -1.721 -0.625 -3.382 -5.096	SU SOU WNS (ns) -0.146 -0.171 -0.182 -0.159 -0.156 -0.156 -0.157 -0.156 -0.157 -0.156 -0.157 -0.158 -0.158 -0.158 -0.158 -0.158 -0.158 -0.158 -0.158 -0.158 -0.160 -0.160 -0.174 -0.140	CE TNS (ns) -26.218 -27.249 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -26.238 -21.549 -21.40 -25.409 -18.943 -23.232 -20.466 -27.070 -19.188 -21.140	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.277 -0.160 -0.200 -0.241 -0.245 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.152 -0.220 -0.299 -0.220 -0.152 -0.160	E2 RO -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -2.005 -2.740 -3.459 -5.755 -1.595 -3.425 -6.548 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.740 -2.934 -2.934 -2.740 -2.934 -2.740 -2.934 -2.934 -2.740 -2.934 -2.934 -2.934 -2.740 -2.934 -2.934 -2.934 -2.740 -2.934 -2.934 -2.934 -2.740 -2.934	SOU SOU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.133 -0.164 -0.159 -0.163 -0.164 -0.178 -0.164 -0.178 -0.164 -0.178 -0.164 -0.174 -0.174 -0.174 -0.174 -0.164 -0.174 -0.164	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -3.692 -3.314 -3.066 -5.307 -3.314
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.01	AST WNS (ns) -0.104 -0.082 -0.127 -0.116 -0.127 -0.116 -0.125 -0.108 -0.125 -0.108 -0.120 -0.153 -0.113 -0.160 -0.125 -0.136 -0.127 -0.136 -0.127 -0.136 -0.127 -0.136 -0.127 -0.136 -0.127 -0.136 -0.127 -0.136 -0.127 -0.130 -0.142 -0.130 -0.127 -0.065 0.147	Ls RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.114 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.177 -2.006 -1.721 -0.625 -3.382 -5.096 -0.304 -0.024 -5.096	SU SOU WNS (ns) -0.146 -0.171 -0.182 -0.158 -0.156 -0.156 -0.157 -0.156 -0.157 -0.156 -0.157 -0.158 -0.156 -0.157 -0.158 -0.143 -0.158 -0.143 -0.158 -0.143 -0.158 -0.143 -0.158 -0.144 -0.143 -0.158 -0.140 -0.140 -0.140 -0.140 -0.140 -0.140 -0.140 -0.140 -0.140 -0.140	CE TNS (ns) -26.218 -27.249 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -25.409 -28.933 -20.466 -27.7070 -19.188 -21.140 -22.411 -22.612 -20.466 -27.070 -19.188 -21.140 -22.411 -22.549 -21.549 -21.549 -21.549 -22.232 -20.466 -27.070 -21.140 -22.411 -22.549 -22.549 -22.546 -27.546 -27.546 -27.546 -21.579 -21.140 -24.322 -20.238 -21.579 -21.140 -24.322 -22.546 -21.140 -24.322 -23.977 -18.991 -26.238 -27.546 -21.140 -26.238 -27.546 -21.140 -26.238 -27.546 -21.140 -26.238 -27.546 -21.140 -26.238 -27.546 -21.140 -26.238 -27.546 -21.140 -26.238 -27.546 -21.140 -25.409 -22.232 -20.466 -27.070 -22.412 -22.947 -22.232 -20.466 -27.070 -22.412 -22.549 -22.232 -20.466 -27.070 -22.412 -22.549 -22.549 -22.549 -22.549 -22.549 -22.540 -22.412 -22.540 -22.412 -22.540 -22.410 -22.54	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.267 -0.274 -0.267 -0.267 -0.267 -0.274 -0.267 -0.160 -0.200 -0.245 -0.277 -0.169 -0.169 -0.173 -0.207 -0.302 -0.229 -0.229 -0.220 -0.152 -0.160 -0.302	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -2.740 -3.459 -3.455 -3.425 -6.548 -2.934 -2.944 -2.845 -2.944 -2.845 -2.944 -2.845 -2.944 -2.845 -2.955 -2.440 -2.845 -2.955 -2.740 -2.845 -2.955 -2.955 -2.845 -2.955 -2.845 -2.955 -2.845 -2.955 -2.955 -2.845 -2.954 -2.955 -2.954 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.954 -2.955 -2.954 -2.955 -2.954 -2.954 -2.954 -2.955 -2.954 -2.954 -2.954 -2.954 -2.955 -2.954 -2.954 -2.954 -2.954 -2.954 -2.954 -2.954 -2.954 -2.954 -2.954 -2.954 -2.955 -2.954 -2.954 -2.954 -2.955 -2.954 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.954 -2.955 -2.955 -2.955 -2.954 -2.955 -2.955 -2.955 -2.954 -2.955 -2.955 -2.955 -2.955 -2.954 -2.955 -2.9	SOU VU SOU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.175 -0.133 -0.164 -0.157 -0.153 -0.163 -0.163 -0.163 -0.164 -0.287 -0.164 -0.2174 -0.164 -0.174 -0.164 -0.174 -0.164 -0.195 -0.164 -0.195 -0.164 -0.129 -0.164 -0.129	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -8.692 -2.940 -2.828 -4.862 -3.066 -5.307 -3.314 -1.549
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.01 0.02	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.124 -0.125 -0.125 -0.126 -0.127 -0.108 -0.209 -0.120 -0.133 -0.113 -0.160 -0.135 -0.113 -0.127 -0.1230 -0.127 -0.065 -0.167 -0.167	Ls RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.114 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.177 -1.721 -0.625 -3.382 -5.096 -0.304 -4.990 -3.904 -4.990	SU SOU WNS (ns) -0.146 -0.171 -0.130 -0.167 -0.158 -0.158 -0.158 -0.156 -0.156 -0.156 -0.156 -0.156 -0.156 -0.156 -0.156 -0.156 -0.156 -0.156 -0.156 -0.157 -0.158 -0.140 -0.143 -0.144 -0.140 -0.140 -0.140 -0.140 -0.141	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -27.489 -21.140 -28.938 -25.584 -27.546 -27.546 -27.546 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -25.409 -8.943 -23.232 -20.466 -27.070 -19.188 -21.140 -22.411 -22.588 -21.549 -22.588 -21.549 -22.588 -21.549 -22.588 -21.549 -22.588 -22.549 -22.588 -22.549 -22.548 -22.549 -22.548 -23.559 -22.548 -23.559 -23.559 -25.549	AST WNS (ns) -0.307 -0.262 -0.271 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.267 -0.160 -0.274 -0.267 -0.160 -0.300 -0.241 -0.245 -0.277 -0.169 -0.169 -0.169 -0.169 -0.200 -0.217 -0.160 -0.302 -0.220 -0.152 -0.160 -0.306	E2 RO -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -2.740 -3.459 -3.425 -6.548 -2.740 -2.845 -5.895 -5.895 -5.881	SO VU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.176 -0.157 -0.163 -0.164 -0.159 -0.163 -0.164 -0.287 -0.164 -0.174 -0.164 -0.174 -0.164 -0.174 -0.174	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.554 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -8.692 -2.940 -3.314 -8.692 -3.3066 -5.307 -3.314 -1.549 -5.932
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.01 0.02 0.03 -3%	AST WNS (ns) -0.104 -0.082 -0.127 -0.116 -0.144 -0.090 -0.125 -0.108 -0.209 -0.127 -0.140 -0.127 -0.140 -0.123 -0.113 -0.113 -0.125 -0.135 -0.114 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.125 -0.136 -0.127 -0.126 -0.126 -0.127 -0.126 -0.127 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.120 -0.127 -0.126 -0.126 -0.127 -0.126 -0.127 -0.126 -0.127 -0.126 -0.127 -0.126 -0.127 -0.126 -0.127 -0.126 -0.126 -0.127 -0.126 -0.126 -0.127 -0.125 -0.136 -0.127 -0.127 -0.125 -0.127 -0.125 -0.127 -0.129 -0.129 -0.149	L: RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.177 -2.006 -1.721 -0.625 -3.382 -5.096 -0.304 -4.990 -3.994 -1.817	SOU SOU WNS (ns) -0.164 -0.171 -0.182 -0.167 -0.178 -0.159 -0.158 -0.140 -0.159 -0.156 -0.137 -0.156 -0.137 -0.150 -0.151 -0.152 -0.140 -0.152 -0.146 -0.147 -0.148 -0.152 -0.146 -0.147 -0.144 -0.144 -0.144	CE TNS (ns) -26,218 -27,249 -27,489 -21,140 -20,008 -28,938 -25,584 -27,546 -28,859 -21,579 -21,140 -24,432 -23,977 -18,991 -26,238 -30,726 -48,136 -21,140 -25,409 -18,943 -23,232 -20,466 -27,070 -19,188 -21,140 -22,411 -22,588 -21,140 -22,584 -21,258	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.267 -0.267 -0.267 -0.186 -0.257 -0.160 -0.267 -0.267 -0.160 -0.300 -0.241 -0.245 -0.277 -0.169 -0.160 -0.302 -0.207 -0.160 -0.2152 -0.160 -0.306 -0.216 -0.216	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -3.425 -6.548 -2.934 -2.934 -2.845 -5.895 -6.801 -2.172	SOU SOU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.157 -0.157 -0.153 -0.164 -0.157 -0.158 -0.168 -0.168 -0.177 -0.164 -0.174 -0.174 -0.174 -0.129 -0.129 -0.228 -0.228	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -8.692 -2.940 -2.828 -3.314 -8.692 -3.314 -3.549 -1.549
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.02 0.03 -3% -2%	AST WNS (ns) -0.104 -0.182 -0.127 -0.116 -0.127 -0.116 -0.127 -0.116 -0.127 -0.116 -0.127 -0.108 -0.209 -0.125 -0.126 -0.127 -0.140 -0.123 -0.136 -0.137 -0.138 -0.125 -0.139 -0.142 -0.230 -0.127 -0.165 -0.127 -0.125 -0.139 -0.142 -0.230 -0.127 -0.065 -0.167 -0.129 -0.149	L: RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.177 -2.006 -1.7721 -0.625 -3.382 -5.096 -0.304 -4.990 -3.994 -3.994 -2.908	SOU SOU WNS (ns) -0.146 -0.171 -0.140 -0.177 -0.178 -0.182 -0.159 -0.156 -0.130 -0.156 -0.137 -0.156 -0.156 -0.150 -0.151 -0.152 -0.140 -0.152 -0.146 -0.152 -0.146 -0.146 -0.152 -0.146 -0.146 -0.146 -0.146 -0.146 -0.146 -0.146 -0.146 -0.146 -0.146 -0.147 -0.148 -0.136	CE TNS (ns) -26.218 -27.249 -27.489 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -66.238 -30.726 -48.136 -21.140 -25.409 -18.943 -23.232 -20.466 -21.140 -25.409 -18.943 -23.232 -20.466 -21.140 -25.849 -21.140 -25.849 -21.140 -25.849 -21.140 -25.238 -21.140 -25.239 -21.140 -25.239 -20.466 -21.140 -22.588 -21.140 -22.322 -20.466 -21.140 -22.588 -21.140 -22.588 -21.140 -22.322 -20.466 -21.140 -22.588 -21.209 -21.209	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.267 -0.267 -0.267 -0.186 -0.257 -0.160 -0.267 -0.274 -0.267 -0.186 -0.277 -0.160 -0.241 -0.245 -0.277 -0.169 -0.160 -0.173 -0.201 -0.152 -0.160 -0.302 -0.216 -0.185 -0.216	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -1.595 -3.425 -6.548 -2.934 -2.934 -5.740 -2.845 -5.895 -6.801 -2.172 -3.382	SOU SOU WNS (ns) -0.174 -0.287 -0.161 -0.287 -0.177 -0.178 -0.163 -0.164 -0.177 -0.176 -0.157 -0.163 -0.164 -0.159 -0.163 -0.164 -0.287 -0.164 -0.233 -0.164 -0.129 -0.129 -0.228 -0.200 -0.239	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -2.681 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.554 -2.817 -2.256 -3.314 -2.554 -2.817 -2.256 -3.314 -2.554 -2.817 -2.256 -3.314 -2.354 -2.817 -2.256 -3.314 -2.354 -2.817 -2.256 -3.314 -2.354 -2.817 -2.256 -3.314 -2.354 -2.817 -2.256 -3.314 -2.354 -2.828 -3.314 -2.554 -2.817 -2.693 -2.403 -3.314 -2.554 -2.693 -2.403 -3.314 -2.554 -2.693 -2.403 -3.314 -2.554 -2.693 -2.403 -3.314 -2.554 -2.693 -2.403 -3.314 -2.554 -2.693 -2.940 -3.314 -2.554 -2.930 -2.930 -3.314 -3.314 -3.314 -3.354 -2.930 -2.403 -3.314 -3.549 -1.549 -1.549 -3.3432 -3.442 -3.442 -3.442 -3.442 -3.442 -3.442 -3.442 -3.442 -3.442 -3.442 -3.442
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.04 -0.05 -0.01 0.02 0.03 -3% -2% -1%	AST WNS (ns) -0.104 -0.082 -0.142 -0.127 -0.116 -0.144 -0.090 -0.125 -0.126 -0.127 -0.160 -0.125 -0.126 -0.127 -0.140 -0.127 -0.140 -0.123 -0.133 -0.135 -0.113 -0.125 -0.135 -0.113 -0.126 -0.137 -0.127 -0.126 -0.139 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.	LS RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.177 -2.006 -1.721 -0.625 -3.382 -5.096 -0.304 -4.990 -3.994 -1.817 -2.908 -0.965 -0.555 -0.565 -0.565 -0.565 -0.565 -0.565 -0.555 -0.565 -0.555 -0.5	SU SO(WNS (ns) -0.164 -0.171 -0.182 -0.167 -0.178 -0.182 -0.159 -0.156 -0.156 -0.156 -0.150 -0.156 -0.150 -0.156 -0.150 -0.158 -0.158 -0.158 -0.158 -0.158 -0.150 -0.140 -0.141 -0.143 -0.158 -0.144 -0.146 -0.146 -0.146 -0.146 -0.141 -0.142 -0.143 -0.144 -0.144 -0.144 -0.144 -0.141	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -25.409 -18.943 -23.232 -20.466 -27.070 -19.188 -21.140 -22.588 -23.951 -19.187 -22.588 -23.951 -9.187 -16.787	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.186 -0.257 -0.160 -0.300 -0.241 -0.245 -0.777 -0.160 -0.173 -0.207 -0.160 -0.173 -0.207 -0.160 -0.173 -0.217 -0.160 -0.302 -0.152 -0.160 -0.306 -0.217 -0.216 -0.185 -0.261 -0.243	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -1.595 -3.425 -6.548 -2.934 -2.740 -2.845 -5.895 -6.801 -2.172 -3.382 -2.361 -2.172 -3.382 -2.361	SOU SOU WNS (ns) -0.174 -0.287 -0.161 -0.287 -0.163 -0.164 -0.176 -0.157 -0.163 -0.164 -0.157 -0.163 -0.164 -0.176 -0.163 -0.164 -0.177 -0.164 -0.174 -0.287 -0.164 -0.174 -0.129 -0.129 -0.228 -0.200 -0.233	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -2.403 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -2.403 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.354 -2.354 -2.354 -2.354 -2.354 -2.354 -2.354 -2.403 -3.314 -2.354 -2.354 -2.354 -2.403 -3.314 -2.554 -3.314 -2.354 -2.354 -2.403 -2.403 -2.403 -2.403 -2.403 -2.403 -2.403 -2.569 -1.191 -2.554 -2.554 -2.403 -2.403 -2.403 -2.554 -2.403 -2.554 -2.403 -2.554 -2.403 -2.403 -2.403 -2.549 -3.314 -3.549 -5.307 -3.314 -3.549 -1.549 -1.549 -3.548 -3.342 -5.5484 -3.384
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio Placement Utilization	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.04 -0.05 -0.01 0.00 0.01 0.02 -1% 0% 10/	AST WNS (ns) -0.104 -0.082 -0.127 -0.116 -0.127 -0.126 -0.125 -0.127 -0.125 -0.127 -0.127 -0.128 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.127 -0.140 -0.127 -0.160 -0.113 -0.125 -0.135 -0.114 -0.127 -0.126 -0.127 -0.127 -0.135 -0.114 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.127 -0.129 -0	Ls. RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -1.721 -0.625 -3.382 -5.096 -0.304 -4.990 -3.994 -1.817 -2.908 -0.965 -5.096	SU SOU WNS (ns) -0.146 -0.171 -0.140 -0.177 -0.178 -0.182 -0.159 -0.156 -0.150 -0.156 -0.150 -0.156 -0.150 -0.150 -0.150 -0.158 -0.158 -0.158 -0.158 -0.158 -0.158 -0.144 -0.146 -0.147 -0.140 -0.141 -0.142 -0.143 -0.144 -0.140 -0.141 -0.142 -0.141 -0.142 -0.141 -0.142 -0.140 -0.141 -0.141 -0.141	CE TNS (ns) -26.218 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -48.136 -21.140 -21.140 -22.411 -22.588 -23.951 -19.187 -31.209 -16.787 -21.140 -21.140 -21.140 -21.140 -22.411 -22.588 -23.951 -19.187 -31.209 -16.787 -21.140 -21.140 -21.140 -21.140 -22.411 -22.588 -23.951 -19.187 -31.209 -16.787 -21.140 -21.140 -21.140 -22.411 -22.588 -23.951 -19.187 -31.209 -16.787 -21.140	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274 -0.267 -0.160 -0.300 -0.245 -0.277 -0.169 -0.169 -0.160 -0.173 -0.2007 -0.302 -0.299 -0.220 -0.152 -0.160 -0.217 -0.216 -0.185 -0.243 -0.160	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.852 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.852 -2.905 -2.740 -3.459 -5.755 -1.595 -1.595 -3.425 -6.548 -2.934 -2.740 -2.845 -5.895 -6.801 -2.172 -3.382 -2.2740 -3.825 -5.895 -6.801 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -3.459 -2.740 -2.174 -3.459 -2.740 -2.172 -3.382 -2.740 -3.455 -3.	SOU SOU WNS (ns) -0.174 -0.287 -0.164 -0.177 -0.164 -0.177 -0.164 -0.178 -0.163 -0.163 -0.163 -0.164 -0.177 -0.163 -0.164 -0.177 -0.163 -0.174 -0.287 -0.161 -0.174 -0.233 -0.164 -0.174 -0.233 -0.164 -0.174 -0.233 -0.161 -0.174 -0.228 -0.200 -0.239 -0.201 -0.164 -0.129 -0.239 -0.201 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.081 -2.554 -2.086 -3.314 -2.554 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.569 -3.314 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.554 -2.086 -3.314 -2.554 -2.554 -2.693 -2.403 -3.314 -2.554
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio Placement Utilization	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.01 0.02 -2% -1% 0% 1%	AST WNS (ns) -0.108 -0.127 -0.127 -0.116 -0.127 -0.116 -0.125 -0.108 -0.209 -0.123 -0.153 -0.113 -0.166 -0.125 -0.135 -0.113 -0.160 -0.125 -0.136 -0.127 -0.160 -0.160 -0.127 -0.160 -0.120 -0.135 -0.114 -0.139 -0.142 -0.230 -0.127 -0.065 -0.167 -0.129 -0.149 -0.129 -0.129 -0.149 -0.127 -0.0965 -0.127 -0.0963 -0.127	Ls. RO TNS (ns) -2.061 -1.735 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -3.382 -5.096 -3.382 -5.096 -0.304 -4.990 -3.994 -1.817 -2.908 -0.965 -5.096 -5.096 -3.213 -4.1313	<i>U</i> <i>SO</i> <i>V</i> <i>V</i> NS (<i>ns</i>) -0.146 -0.164 -0.171 -0.140 -0.130 -0.167 -0.178 -0.159 -0.159 -0.158 -0.140 -0.156 -0.130 -0.156 -0.130 -0.156 -0.158 -0.143 -0.158 -0.143 -0.158 -0.144 -0.158 -0.140 -0.140 -0.140 -0.158 -0.140 -0.140 -0.140 -0.158 -0.140	CE TNS (ns) -26.218 -27.249 -27.489 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -23.977 -18.991 -26.238 -21.140 -25.284 -23.977 -18.991 -26.238 -21.140 -25.284 -21.140 -25.284 -21.140 -25.284 -21.140 -25.284 -21.140 -25.284 -21.140 -25.284 -21.140 -21.140 -21.140 -25.284 -21.140 -20.466 -21.140 -20.466 -21.140 -22.411 -22.588 -23.951 -19.187 -21.140 -20.818 -21.140 -20.818 -27.270 -21.140 -20.818 -27.270 -21.140 -20.818 -27.270 -21.140 -20.818 -27.270 -27.140 -20.818 -27.270 -27.140 -20.818 -27.270 -27.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -27.2707 -21.140 -20.818 -21.297 -21.140	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274 -0.267 -0.160 -0.300 -0.2201 -0.245 -0.277 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.160 -0.207 -0.200 -0.216 -0.160 -0.217 -0.216 -0.185 -0.261 -0.189 -0.160 -0.189 -0.218	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -1.595 -3.425 -5.548 -2.934 -2.740 -2.845 -5.895 -6.548 -2.934 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.895 -6.548 -2.740 -2.845 -5.740 -2.845 -5.755 -1.595 -3.822 -2.740 -2.845 -5.755 -1.595 -3.822 -2.740 -2.934 -2.740 -2.935 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.740 -2.936 -2.9	SOU SOU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.163 -0.163 -0.164 -0.157 -0.163 -0.164 -0.159 -0.163 -0.164 -0.287 -0.161 -0.174 -0.233 -0.164 -0.129 -0.228 -0.200 -0.239 -0.201 -0.164 -0.188 -0.201	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314 -2.854 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314 -2.817 -2.256 -1.191 -2.549 -2.403 -3.314
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio Placement Utilization	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.01 0.02 0.03 -3% -2% -1% 0% 1% 2% 3%	AST WNS (ns) -0.108 -0.127 -0.116 -0.125 -0.126 -0.127 -0.116 -0.127 -0.116 -0.125 -0.108 -0.209 -0.120 -0.153 -0.113 -0.166 -0.125 -0.136 -0.127 -0.136 -0.125 -0.136 -0.127 -0.160 -0.135 -0.114 -0.139 -0.142 -0.230 -0.127 -0.065 -0.167 -0.129 -0.149 -0.127 -0.0983 -0.127 -0.096 -0.123 -0.123	Ls. RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -3.970 -1.177 -2.066 -3.382 -5.096 -0.304 -4.990 -3.994 -1.817 -2.908 -0.965 -5.096 -3.213 -6.897	SU SOU WNS (ns) -0.146 -0.171 -0.182 -0.159 -0.156 -0.156 -0.157 -0.158 -0.156 -0.157 -0.158 -0.150 -0.151 -0.152 -0.143 -0.158 -0.158 -0.158 -0.158 -0.158 -0.143 -0.158 -0.143 -0.158 -0.144 -0.144 -0.133 -0.144 -0.134 -0.144 -0.144 -0.144 -0.140 -0.141 -0.142 -0.143 -0.144 -0.133 -0.140	CE TNS (ns) -26.218 -27.249 -27.249 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -21.5409 -26.238 -21.140 -25.409 -18.943 -23.232 -20.466 -27.070 -19.188 -21.140 -22.411 -22.588 -21.140 -22.588 -21.140 -22.588 -21.140 -22.588 -21.140 -22.588 -21.140 -22.588 -21.140 -22.588 -21.140 -22.518 -19.187 -31.209 -6.27.267 -25.518	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274 -0.267 -0.160 -0.300 -0.220 -0.245 -0.277 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.169 -0.160 -0.207 -0.216 -0.152 -0.160 -0.216 -0.216 -0.216 -0.218 -0.218	E2 RO -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -1.595 -3.425 -6.548 -2.934 -2.172 -3.382 -2.172 -3.382 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.740 -2.172 -3.382 -2.292 -6.533 -6.548 -2.740 -2.172 -3.382 -2.292 -6.548 -2.740 -	SOU VU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.176 -0.157 -0.133 -0.164 -0.159 -0.163 -0.164 -0.178 -0.164 -0.174 -0.164 -0.174 -0.164 -0.129 -0.200 -0.239 -0.201 -0.164 -0.188 -0.209 -0.201	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -3.666 -5.307 -3.314 -1.549 -5.932 -3.432 -5.484 -3.314 -2.548 -3.314 -5.932 -3.432 -5.484 -3.314 -2.548 -3.314 -5.932 -3.432 -5.484 -3.314 -2.548 -3.314 -5.932 -3.432 -5.484 -3.314 -2.548 -3.314 -5.932 -3.432 -5.484 -3.314 -5.932 -3.432 -5.484 -3.314 -5.548 -5.547 -5.932 -3.432 -5.484 -3.314 -5.548 -5.547 -5.932 -3.314 -5.549 -5.547 -5.932 -3.314 -5.549 -5.932 -5.484 -5.548 -5.547 -5.548 -5.547 -5.932 -5.484 -5.548 -5.547 -5.548 -5.307 -5.932 -5.484 -5.548 -5.547 -5.548 -5.307 -5.932 -5.484 -5.314 -5.548 -5.547 -5.932 -5.484 -5.548 -5.547 -5.548 -5.547 -5.932 -5.484 -5.548 -5.557 -5.548 -5.557 -5.548 -5.548 -5.557 -5.548 -5.548 -5.557 -5.548 -5.548 -5.557 -5.548 -5.557 -5.548 -5.557 -5.548 -5.557 -5.568 -5.557 -5.548 -5.557 -5.568 -5.557 -5.568 -5.557 -5.568 -5.557 -5.568 -5.557 -5.568 -5.557 -5.568 -5.557 -5.568 -5.558
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio Placement Utilization Best	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps -3ps -3ps -3ps -3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -3ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.01 0.02 -1% 0% 1% 2% 3%	AST WNS (ns) -0.104 -0.082 -0.127 -0.116 -0.127 -0.116 -0.127 -0.116 -0.125 -0.108 -0.125 -0.131 -0.125 -0.136 -0.127 -0.136 -0.127 -0.139 -0.140 -0.127 -0.136 -0.127 -0.136 -0.127 -0.136 -0.127 -0.139 -0.140 -0.127 -0.065 -0.167 -0.129 -0.129 -0.149 -0.129 -0.127 -0.083 -0.127 -0.083 -0.127 -0.023 -0.127 -0.023 -0.129 -0.123 -0.	Ls RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -5.096 -2.970 -1.721 -0.625 -3.382 -5.096 -0.304 -4.990 -3.994 -1.817 -2.908 -0.3213 -4.0897 -2.813	SU SOU WNS (ns) -0.146 -0.171 -0.182 -0.158 -0.156 -0.156 -0.157 -0.158 -0.156 -0.157 -0.156 -0.157 -0.158 -0.150 -0.156 -0.150 -0.156 -0.152 -0.140 -0.152 -0.140 -0.158 -0.140 -0.158 -0.143 -0.150 -0.144 -0.160 -0.174 -0.140 -0.128 -0.141 -0.130 -0.141 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164 -0.164<	CE TNS (ns) -26.218 -27.249 -27.249 -27.249 -27.249 -27.489 -21.140 -20.008 -28.938 -25.584 -27.546 -28.859 -21.579 -21.140 -24.432 -23.977 -18.991 -26.238 -30.726 -21.140 -25.409 -28.933 -20.466 -27.070 -19.188 -21.140 -22.411 -22.588 -21.140 -22.411 -22.588 -21.140 -22.411 -22.588 -21.140 -22.411 -22.588 -21.140 -20.818 -21.558 -21.140 -20.818 -25.558	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.237 -0.267 -0.274 -0.267 -0.274 -0.267 -0.274 -0.267 -0.160 -0.300 -0.220 -0.245 -0.277 -0.169 -0.173 -0.207 -0.169 -0.169 -0.173 -0.207 -0.169 -0.169 -0.169 -0.169 -0.169 -0.160 -0.302 -0.216 -0.185 -0.261 -0.185 -0.218 -0.2152	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -2.740 -3.459 -2.740 -3.459 -2.740 -2.925 -3.425 -6.548 -2.934 -2.934 -2.845 -5.895 -6.801 -2.172 -3.382 -2.361 -2.740 -1.091 -5.300 -1.091	SOU VU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.176 -0.157 -0.163 -0.164 -0.159 -0.163 -0.164 -0.174 -0.287 -0.161 -0.174 -0.287 -0.164 -0.129 -0.200 -0.239 -0.201 -0.164 -0.188 -0.209 -0.200 -0.239 -0.201 -0.240	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.354 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -8.692 -2.828 -4.862 -3.066 -5.307 -3.314 -1.549 -5.932 -3.432 -5.484 -4.398 -3.314 -2.5484 -2.817 -2.256 -1.191 -2.693 -2.403 -3.314 -2.828 -3.314 -1.549 -5.932 -3.432 -5.484 -3.314 -2.5484 -3.314 -1.549 -5.932 -3.432 -5.484 -3.314 -2.5484 -3.314 -1.549 -5.932 -3.432 -5.484 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -5.548 -3.314 -1.549 -3.314 -2.106 -3.114 -1.549 -3.314 -2.106 -3.114 -1.549 -3.114 -1.549 -3.314 -3.114 -1.549 -3.314 -1.549 -3.314 -1.549 -3.314 -1.549 -3.314 -1.549 -3.314 -1.549 -3.314 -3.14 -1.549 -3.14 -1.549 -3.14 -1.549 -3.14 -1.549 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.14 -3.15 -1.191
Parameter Clock Cycle Clock Uncertainty IO Delay Aspect Ratio Placement Utilization Best Worst	Noise (Δ) -3ps -2ps -1ps 0ps 1ps 2ps -3ps -2ps -1ps 0ps 1ps 2ps -1ps 0ps 1ps 2ps -1ps 0ps 1ps 2ps -2ps -1ps 0ps 1ps 2ps 3ps -0.03 -0.02 -0.01 0.00 0.01 0.02 0.03 -3% -2% -1% 0% 3%	AST WNS (ns) -0.104 -0.082 -0.127 -0.116 -0.127 -0.116 -0.127 -0.116 -0.127 -0.116 -0.127 -0.108 -0.209 -0.125 -0.108 -0.127 -0.140 -0.125 -0.136 -0.137 -0.160 -0.139 -0.142 -0.230 -0.142 -0.127 -0.165 -0.167 -0.127 -0.065 -0.167 -0.129 -0.149 -0.129 -0.149 -0.127 -0.065 -0.128 -0.129 -0.149 -0.123 -0.100 -0.065 -0.230	L: RO TNS (ns) -2.061 -1.298 -3.539 -5.096 -1.735 -3.611 -1.508 -4.246 -0.507 -1.674 -5.096 -3.462 -2.813 -6.908 -2.114 -1.401 -0.728 -3.096 -2.970 -1.177 -2.006 -1.721 -0.625 -3.382 -5.096 -0.304 -4.990 -3.994 -1.817 -2.908 -0.965 -3.213 -4.113 -0.897 -2.813 -6.908	SU SOU WNS (ns) -0.164 -0.171 -0.182 -0.167 -0.159 -0.158 -0.159 -0.156 -0.130 -0.158 -0.159 -0.156 -0.137 -0.156 -0.137 -0.150 -0.151 -0.152 -0.140 -0.152 -0.140 -0.152 -0.146 -0.152 -0.146 -0.147 -0.148 -0.136 -0.144 -0.139 -0.164 -0.139 -0.164 -0.134	CE TNS (ns) -26,218 -27,249 -27,489 -21,140 -20,008 -28,938 -25,584 -27,546 -28,859 -21,579 -21,140 -24,432 -23,977 -18,991 -26,238 -30,726 -48,136 -21,140 -25,409 -18,943 -23,232 -20,466 -27,070 -19,188 -23,951 -19,187 -31,209 -16,787 -21,140 -20,818 -27,267 -25,518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,55518 -27,5578 -27,55518 -27,555518 -27,555518 -27,555518 -27,555518 -27,555518 -27,555518 -27,555518 -27,555518 -27,555518 -27,555518 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,5555 -27,555 -27	AST WNS (ns) -0.307 -0.262 -0.271 -0.160 -0.267 -0.274 -0.267 -0.186 -0.257 -0.160 -0.267 -0.160 -0.200 -0.241 -0.245 -0.277 -0.160 -0.160 -0.160 -0.160 -0.202 -0.152 -0.160 -0.216 -0.216 -0.216 -0.241 -0.220 -0.152 -0.160 -0.216 -0.216 -0.216 -0.218 -0.218 -0.221 -0.307	E2 RO TNS (ns) -1.945 -2.472 -3.869 -2.740 -2.084 -3.992 -7.430 -1.510 -1.424 -4.424 -4.424 -2.740 -3.832 -2.292 -6.533 -6.694 -4.769 -2.905 -2.740 -3.459 -5.755 -1.595 -3.425 -6.548 -2.934 -2.934 -2.845 -5.895 -3.825 -6.548 -2.934 -2.845 -5.895 -3.825 -6.548 -2.934 -2.740 -2.845 -5.895 -3.382 -2.361 -2.740 -2.845 -5.300 -1.091 -6.299 -5.300 -1.091 -7.430	SOU SOU WNS (ns) -0.174 -0.161 -0.287 -0.164 -0.177 -0.178 -0.096 -0.157 -0.153 -0.164 -0.157 -0.163 -0.164 -0.176 -0.168 -0.168 -0.174 -0.164 -0.174 -0.129 -0.128 -0.228 -0.200 -0.239 -0.201 -0.164 -0.239 -0.201 -0.164 -0.228 -0.200 -0.228 -0.200 -0.228 -0.200 -0.228 -0.228 -0.228 -0.287	CE TNS (ns) -2.828 -2.940 -8.692 -3.314 -2.403 -2.693 -1.191 -2.681 -2.554 -2.086 -3.314 -2.554 -2.086 -3.314 -2.554 -2.817 -2.256 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.693 -2.403 -3.314 -2.554 -2.828 -3.314 -3.314 -3.314 -3.314 -3.549 -1.549 -5.331 -5.484 -3.314 -5.583 -5.484 -3.314 -5.484 -3.314 -5.693 -5.484 -3.314 -5.693 -5.484 -5.3314 -5.693 -5.484 -5.3314 -5.693 -5.484 -5.3314 -5.693 -5.484 -5.3314 -5.693 -5.588 -5.314 -5.693 -5.484 -5.314 -5.693 -5.484 -5.566 -5.314 -5.693 -5.484 -5.566 -5.567 -1.191 -6.203 -6.156 -1.191 -8.692

TABLE VI

Rank order (with respect to expected best-of-k solution quality from 100 trials, for five input parameters of perturbations, for k = 1,..., 10 runs. This table is derived from *AES* results implemented using *ASTRO*.

		Al	ES					JPI	EG						
k	T	S	B	A	U	k	T	S	B	A	U				
1	1	3	2	4	5	1	4	2	5	3	1				
2	2	3	1	4	5	2	4	2	5	3	1				
3	1	3	2	4	5	3	4	2	5	3	1				
4	2	3	1	4	5	4	4	2	5	3	1				
5	2	3	1	4	5	5	4	2	5	3	1				
6	1	3	2	4	5	6	5	2	4	3	1				
7	1	3	2	4	5	7	5	2	4	3	1				
8	2	3	1	4	5	8	5	2	4	3	1				
9	1	3	2	4	5	9	5	2	4	3	1				
10	1	3	2	4	5	10	5	3	4	2	1				
											$ \begin{array}{c} U \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 3 \\ 3 \\ 3 \\ 3 \\ 3 \\ 3 \\ 3 \\ 1 \\ $				
	1	LS	SU			<u> </u>		ΕX	U						
k	T		SU B	A	U	k	Т	EX S	U B	A	U				
k1	<i>T</i> 2	<i>LS</i> <i>S</i> 4	SU B 3	A 5	U 1	k 1	<i>T</i> 5	<i>ЕХ</i> <i>S</i> 4	TU B 1	A 2	U 3				
k 1 2	T 2 1	<i>LS</i> <i>S</i> 4 3	SU B 3 4	A 5 5	U 1 2	k 1 2	T 5 5	EX S 4 4	<i>TU</i> <i>B</i> 1 2	A 2 1	U 3 3				
	T 2 1 1	<i>LS</i> <i>S</i> 4 3 4	SU B 3 4 5	A 5 5 3	U 1 2 2	$\begin{array}{c} k \\ 1 \\ 2 \\ 3 \end{array}$	T 5 5 5	<i>EX</i> <i>S</i> 4 4 3	TU B 1 2 1	A 2 1 2	U 3 3 4				
$ \begin{array}{c} k\\ 1\\ 2\\ 3\\ 4 \end{array} $	<i>T</i> 2 1 1 2	LS S 4 3 4 4 4	SU B 3 4 5 5	A 5 5 3 3	U 1 2 2 1	$\begin{array}{c} k\\ 1\\ 2\\ 3\\ 4 \end{array}$	<i>T</i> 5 5 5 5 5		TU B 1 2 1 2	A 2 1 2 1	U 3 3 4 3				
$ \begin{array}{c} k\\ 1\\ 2\\ 3\\ 4\\ 5 \end{array} $	$\begin{array}{c c} T \\ 2 \\ 1 \\ 1 \\ 2 \\ 1 \end{array}$	$ \begin{array}{c c} LS\\ S\\ 4\\ 3\\ 4\\ 4\\ 4\\ 4 \end{array} $	SU B 3 4 5 5 5 5	A 5 5 3 3 3	U 1 2 2 1 2	$\begin{array}{c c} k \\ \hline 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array}$	T 5 5 5 5 5 5	<i>EX</i> <i>S</i> 4 3 4 3	TU B 1 2 1 2 2	A 2 1 2 1 1 1	U 3 3 4 3 4 3 4				
	$\begin{array}{c c} T \\ 2 \\ 1 \\ 1 \\ 2 \\ 1 \\ 3 \end{array}$	$ \begin{array}{c c} LS\\ S\\ 4\\ 3\\ 4\\ 4\\ 4\\ 4\\ 4 \end{array} $	<i>SU</i> <i>B</i> 3 4 5 5 5 5 5 5	A 5 5 3 3 3 1	U 1 2 1 2 1 2 2	$\begin{array}{c c} k \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{array}$	<i>T</i> 5 5 5 5 5 5 5 5	<i>EX</i> <i>S</i> 4 4 3 4 3 3	TU B 1 2 1 2 2 2 2	A 2 1 2 1 1 1 1	U 3 3 4 3 4 4 4				
$ \begin{array}{c} k\\ 1\\ 2\\ 3\\ 4\\ 5\\ 6\\ 7 \end{array} $	$\begin{array}{c} T\\ 2\\ 1\\ 1\\ 2\\ 1\\ 3\\ 3\end{array}$	$ \begin{array}{c c} LS\\ \hline S\\ \hline 4\\ \hline 3\\ \hline 4\\ \hline 4\\ \hline 4\\ \hline 4\\ \hline 4\\ \hline 4$	<i>SU</i> <i>B</i> 3 4 5 5 5 5 5 5 5 5	$ \begin{array}{r} A \\ 5 \\ $	U 1 2 2 1 2 2 2 2	$\begin{array}{c c} k \\ \hline 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ \end{array}$	T 5 5 5 5 5 5 5 5 5 5 5	<i>EX</i> <i>S</i> 4 4 3 4 3 4 3 4	TU B 1 2 1 2 2 2 2 2	$ \begin{array}{c} A \\ 2 \\ 1 \\ 2 \\ 1 \\ 1 \\ 1 \\ 1 \end{array} $	U 3 3 4 3 4 4 3 4 4 3				
k 1 2 3 4 5 6 7 8	T 2 1 1 2 1 3 3 3 3	$ \begin{array}{c c} LS\\ \hline S\\ \hline 4\\ \hline 3\\ \hline 4\\ \hline 4\\ \hline 4\\ \hline 4\\ \hline 4\\ \hline 4$	<i>SU</i> <i>B</i> 3 4 5 5 5 5 5 5 5	$ \begin{array}{r} A \\ 5 \\ $	U 1 2 2 1 2 2 2 2 2 2	k 1 2 3 4 5 6 7 8	<i>T</i> 5 5 5 5 5 5 5 5 5 5 5	$ \begin{array}{c} EX\\ S\\ 4\\ 4\\ 3\\ 4\\ 3\\ 4\\ 4\\ 4 \end{array} $	U B 1 2 1 2 2 2 2 2 2 2	A 2 1 2 1 1 1 1 1 1	U 3 3 4 3 4 3 4 3 3				
	$ \begin{array}{c} T \\ 2 \\ 1 \\ 1 \\ 2 \\ 1 \\ 3 \\ 3 \\ 2 \\ \end{array} $	$ \begin{array}{c c} LS\\ \hline S\\ \hline 4\\ 3\\ 4\\ 4\\ 4\\ 4\\ 4\\ 4\\ 4\\ 4\\ 4\\ 4\\ 4\\ 5\\ \hline 6\\ \hline 6\\ \hline 7\\ \hline 8\\ \hline 8\\ \hline 8\\ \hline 8\\ \hline 8\\ \hline 8\\ \hline 8$	<i>SU</i> <i>B</i> 3 4 5 5 5 5 5 5 5 5 5	$ \begin{array}{r} A \\ 5 \\ $	U 1 2 2 1 2 2 2 2 2 3	k 1 2 3 4 5 6 7 8 9	<i>T</i> 5 5 5 5 5 5 5 5 5 5 5 5		U B 1 2 1 2 2 2 2 2 2 2 2 2 2	$ \begin{array}{c} A \\ 2 \\ 1 \\ 2 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{array} $	U 3 4 3 4 4 3 4 4 3 3 3				

all simulation results that were summarized in Table V.

First, we find which input parameter is the most useful to perturb, with respect to k = 1, 2, 3, ..., 10. We randomly choose k solutions in each of 100 trials, out of our seven different runs for each perturbed input parameter: clock cycle time (T), clock uncertainty (S), input/output delay (B), aspect ratio (A), and utilization (U). We then find worst, best, and average of the best WNS from 100 trials for each k value.

Table VI shows the "quality" ranks of each input parameter for our testcases implemented using *ASTRO*. From the table, we observe that clock cycle time (*T*) or input/output delay (*B*) perturbations may be the best for the *AES* design, utilization (*U*) perturbation may be the best for the *JPEG* design, and input/output delay (*B*) or aspect ratio (*A*) perturbations may be the best for the *EXU* design. For *LSU*, when *k* is small, clock cycle time (*T*) or utilization (*U*) perturbations give the best design quality, but when *k* is larger than six, aspect ratio (*A*) perturbations give the best design quality.

Second, we find the best k value if both the input parameters and the parameter values are randomly chosen, since the best knob is not common for different testcases. For each testcase, we randomly choose k solutions in each of 100 trials, out of the 35 different solutions available (five different input parameters times seven different (perturbed) values of each parameter) for the testcase. Figures 4, 6, 8, and 10 (one figure per testcase) show the worst, best and average WNS values out of 100 trials of best-of-k sampling when *ASTRO* is used for implementation. Figures 5, 7, 9, and 11 show the worst, best and average WNS values out of 100 trials of best-of-ksampling when *SOCE* is used for implementation.

From Figures 4-11, we observe that the average WNS from 100 trials improves rapidly with increasing *k*. In most cases, when k = 3, the average expected quality is within 20*ps* of the best solution quality. We also observe that the worst-case WNS from 100 trials can be improved significantly with small *k*. For

example, when k = 3, multi-run or multi-start using *SOCE* is expected to improves WNS of *EXU* by more than 100ps.⁴



Fig. 4. Worst, best and average WNS values out of 100 trials with respect to expected best-of-*k* solution quality: *AES* implemented using *ASTRO*.



Fig. 5. Worst, best and average WNS values out of 100 trials with respect to expected best-of-k solution quality: *AES* implemented using *SOCE*.



Fig. 6. Worst, best and average WNS values out of 100 trials with respect to expected best-of-k solution quality: *JPEG* implemented using *ASTRO*.

IV. CONCLUSION

In this work, we have experimentally assessed the nature of 'chaotic' behavior in commercial IC implementation tools. 'Chaos' is attributable to miscorrelations of performance analyses between synthesis and P&R, and between P&R

⁴With the multi-run scenario, the runtime overhead of k = 3 can be naively viewed as three times larger than that of the traditional design methodology. However, if we consider the effort and time required to analyze and manually improve timing quality by more than 100 ps, the overhead from the pure tool runtime can be substantially compensated. Furthermore, since better quality of the initial optimization typically results in faster timing closure, the overall design cycle time can be potentially reduced. With the multi-start scenario, it is clear that there will be negligible design time overhead, since our methodology can be trivially implemented and does not require any change to the existing design flow.



Fig. 7. Worst, best and average WNS values out of 100 trials with respect to expected best-of-k solution quality: *JPEG* implemented using *SOCE*.



Fig. 8. Worst, best and average WNS values out of 100 trials with respect to expected best-of-k solution quality: LSU implemented using ASTRO.



Fig. 9. Worst, best and average WNS values out of 100 trials with respect to expected best-of-*k* solution quality: *LSU* implemented using *SOCE*.



Fig. 10. Worst, best and average WNS values out of 100 trials with respect to expected best-of-*k* solution quality: *EXU* implemented using *ASTRO*.



Fig. 11. Worst, best and average WNS values out of 100 trials with respect to expected best-of-*k* solution quality: *EXU* implemented using *SOCE*.

and signoff. We also characterize the effects of intentional, negligible perturbations of input parameters on output quality of commercial tools and flows.

Based on our experimental results, we propose a methodology to exploit the chaotic tool behavior using 'multi-run' (1 license or 1 CPU scenario) or 'multi-start' (multiple licenses and CPUs scenario) with intentional perturbations of the input parameters. We also describe an efficient method to determine the best number k of multiple runs that will yield predictably high-quality solutions without any additional manual analysis or manipulation, without changing any design flows, and without wasting valuable computing resources.

The deployment of new implementation and signoff tool capabilities opens up new directions for ongoing and future work, including the following. (1) We seek to analyze the potential advantages of the inherent "chaos" in advanced *physical synthesis* tools that exploit physical information at the synthesis stage to reduce synthesis-placement miscorrelations. (2) We seek to evaluate the benefits of chaos in conjunction with more advanced signoff methodologies (e.g., signal integrity-enabled STA), as well as more advanced signoff analyses (e.g., path-based analysis), which may exhibit even more chaotic behavior than today's standard flows.

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