Is Overlay Error More Important Than Interconnect Variations in Double Patterning?

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ABSTRACT

Double patterning lithography seems to be a prominent choice for 32*nm* and 22*nm* technologies. Double patterning lithography techniques require additional masks for a single interconnect layer. Consequently, mask shift-induced overlay errors introduce additional variability into interconnect coupling capacitances. An important open question is whether overlay-induced performance impacts are more significant than performance variations caused by variability in interconnects. We provide TCAD as well as chip-level analyses to determine whether overlay error should receive more attention than interconnect variations during interconnect manufacturing. We develop conclusions to help determine which component should be given more importance in specific double patterning process variants.

Categories and Subject Descriptors

B.7.2 [**INTEGRATED CIRCUITS**]: Design Aids—*Simulation*

General Terms

Design, Experimentation, Verification

Keywords

overlay, double patterning lithography, interconnect variations

1. INTRODUCTION

Stringent printability requirements of sub-45*nm* interconnect features have led the industry to consider double patterning lithography. The transition from 248*nm* to 193*nm* wavelength lithography sources has been cost effective; however, the transition from 193*nm* to 157*nm* or EUV sources seems more costly than double patterning using a 193*nm* source. There are three commonly known types of double patterning [1]. These are double exposure (DE), double patterning (DP) and spacer double patterning (SDP). In DE, two lithography steps are followed by a single etch step.[1] In DP, two lithography and etch steps are used. Finally in SDP, one lithography and one etch step are followed by spacer formation, oxide deposition, chemical-mechanical polishing and a second etch. SDP is seen as a very viable option for regular patterns such as poly gates [4] as well as bitlines [5] of a memory design. However, SDP requires additional process steps, including chemical-mechanical polishing which may be costly and difficult to optimize, and also requires a trim mask to remove undesired spacer (trimming) or generated patterns (repairing) when implementing irregular patterns [4], [6].

Overlay error with double patterning may be a limiting performance factor. As there is more than one mask per layer for which double patterning is applied[2], mask misalignment becomes a problem. For SDP, instead of mask misalignment, spacer thickness determines an important part of the overlay error. Overlay error is a function of process parameters such as mask misalignment, material stress-impacted deformations, lithography- and etch-impacted topography differences, and lens aberrations. Mask misalignments are a major factor in overlay and we therefore focus on them in this paper. Excessive mask shift-induced overlay errors may also result in reliability problems such as open vias. Such problems reduce yield. When such issues are not present, there will be variability issues.

For all these processes, either positive or negative(-tone) photoresist (PR) can be an option. Under overlay errors, positive PR will have critical dimension (CD) variations of patterns on the photoresist while negative PR will have pitch variations of patterns on the photoresist. With a trench-first interconnect process, a dielectric trench is first etched, metal is deposited and chemical-mechanical polishing is applied for each interconnect layer. Hence, for interconnects, DE or DP with positive (negative) photoresist results in pitch (width) variations for interconnects, in contrast to the patterns on the photoresist after exposure. SDP with positive PR results in width variations, whereas SDP with negative PR results in width and pitch variations.

Another choice in double patterning is the reference for alignment. There are two options [18].

- **Indirect alignment (IA).** Both masks for a given layer are aligned with respect to a third layer underneath, with similar overlay error (*S*) as a single patterning process, as shown in Figure 1(a). However, the standard deviation of overlay errors between double patterning masks can increase by a square root of two factor, due to the statistical (RSS) summation of two independent overlay errors.

- **Direct alignment (DA).** The second mask for a given layer is aligned with respect to the first mask of the same layer

[1]As a variant of DE, litho-freeze litho-etch (LFLE) process is developed to reduce the interference between the first and the second resist [2], [3].

[2]Even though SDP may not require additional masks, it requires certain sacrificial materials, such as oxides, used as masks.

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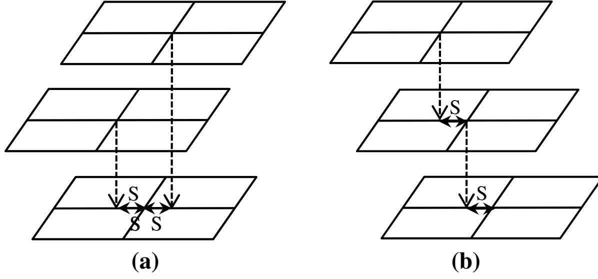


Figure 1: Alignment methodologies. (a) Indirect alignment (IA). (b) Direct alignment (DA).

as shown in Figure 1(b). While this alignment methodology reduces standard deviation of overlay errors by about 30% ($1 - 1/\sqrt{2}$) compared with IA, it brings additional difficulties in optimizing the process parameters for the second mask alignment to the first mask [18].

In this paper, we compare the impact of the additional interconnect variability source "overlay error" that arises in double patterning with the impact of other traditional interconnect variability sources. In the rest of the paper, in Section II, we briefly go over the literature on interconnect variational analysis. In Section III, we characterize overlay error and interconnect variation impact on coupling capacitances in a double patterning process using TCAD simulations. In Section IV, we extend our analysis framework to full-chip performance analysis. Section V presents experimental results for a hypothetical 45*nm* technology. We conclude our paper in Section VI.

2. PREVIOUS WORK

Interconnect performance in the presence of process variations has been analyzed in a number of papers. Wang et al. [7] have used Hilbert-space and orthogonal polynomial expansions for stochastic analysis of interconnects. Nakagawa et al. [8] have introduced models for dielectric thickness variation induced by pattern dependency of the chemical-mechanical polishing and metal width variation due to lithography bias. Shigyo et al. [9] have shown that there is a trade-off between C and RC delay variations due to the fringing capacitance and have proposed design guidelines to reduce variations. Lin et al. [10] have used sensitivity analysis to relate delay to interconnect dimensions.

As interconnect performance is projected to increasingly dominate circuit delay, improved comprehension of interconnect variation impacts offers significant possibility for relaxation of design constraints. Techniques have been presented to account for these variations. Nagaraj et al. [11] have considered interconnect variations in cross-talk verification. Venkatraman et al. [12] have investigated interconnect variation effects for multi-level signaling. Capacitance extraction under process variations has been proposed by Labun et al. [13]. Lu et al. [14] have presented a statistical corner analysis methodology for interconnects. Kahng et al. [15] have conducted field solver analysis to generate additional interconnect matching rules to help reduce design pessimism. Eichelberger et al. [16] conduct variance analysis with respect to wafer exposure and develop higher-order models.

Additional literature seeks to quantify the impact of overlay error via analytical and empirical analysis. Wakamoto et al. [17] propose an on-the-fly overlay error correction mechanism. Laidler et al. [18] identify error sources in overlay. Kim et al. [19] present silicon results of 193nm double patterning using negative-tone photoresist. Sezginer et al. [20] propose a graphical method of visualizing the many-dimensional process window for double patterning considering width and space variation from overlay. The coupling and total capacitance changes from overlay error in back end of line (BEOL) double patterning process is studied with TCAD simulations in [21]. Yang et al. [22] present timing variation from overlay error in double patterning with analytical modeling of overlay error and capacitance variation from the overlay error. Ghaida et al. [23] quantify the impact of each overlay error source through modeling of the capacitance variation for each overlay error component, and observe that translational overlay error is the largest component of the capacitance variation. However, impacts on full-chip capacitance and timing have not been discussed in the literature, and neither have the SDP technology option or the full taxonomy of alignment types.

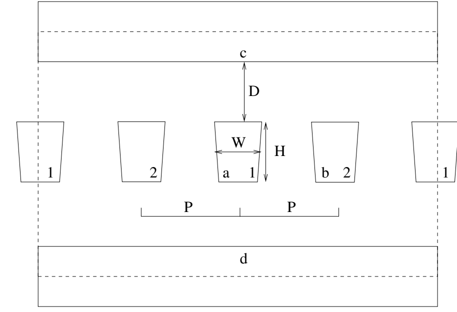


Figure 2: Three interconnect layers shown. Side view. W, H, D and P are the parameters affecting variability in coupling capacitance. Coupling capacitances between interconnect a and interconnects b, c and d are reported in a capacitance table. Interconnects decomposed into mask1 and mask2.

3. INTERCONNECT ANALYSIS

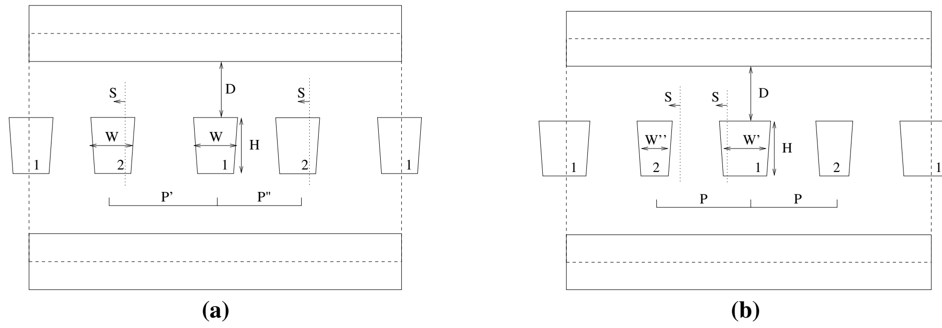
Designers utilize capacitance tables from design manuals during circuit design. Capacitance tables are generated using two- or three-dimensional field solver simulations for various width and spacing combinations of interconnects per each interconnect layer. Due to design differences such as density variations and process variations, interconnect and dielectric widths and heights may vary. Hence, we provide variational capacitance tables. Given statistical variation information per each width and height by the fab, we generate worst-case corners for each coupling capacitance. Next, we describe a variational methodology for a traditional (single patterning) lithography process.

3.1 Traditional Process

Figure 2 shows a side view of three layers of interconnects. Interconnect width (W), height (H), dielectric height (D) and pitch (P) are indicated. The coupling capacitances of interest are the intralayer coupling capacitance $C^{intra} = C^{ab}$, upper interlayer coupling capacitance $C^{up} = C^{ac}$ and the lower interlayer coupling capacitance $C^{down} = C^{ad}$. We use the design of experiments (DOE) given below for regular interconnect variational analysis.

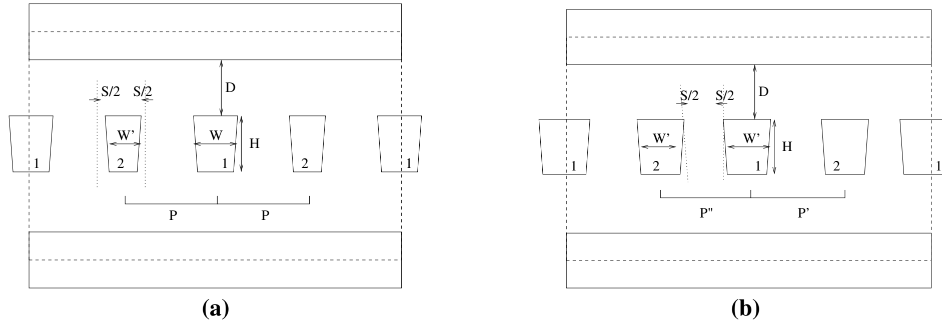
1. **for** (i =-3,$i \leq$3,$i = i$+1) {
2. **for** (j =-3,$j \leq$3,$j = j$+1) {
3. **for** (k =-3,$k \leq$3,$k = k$+1) {
4. W=W_{nom}+i*$W_{1\sigma}$
5. H=H_{nom}+j*$H_{1\sigma}$
6. D=D_{nom}+k*$D_{1\sigma}$
7. Run field solver over parameterized structure.}}}
8. Find nominal and worst-case conditions for each coupling.

The enumerators i, j and k are used to set the interconnect width, height and dielectric height to their -3σ, nominal (nom) and $+3\sigma$



(a) **(b)**

Figure 3: Three interconnect layers shown. Side view. $P" \leq P \leq P'$ and $W" \leq W \leq W'$. (a) In a positive photoresist process, interconnects printed using mask 2 are shifted by S due to overlay error, thereby causing additional variability in coupling capacitances. (b) In a negative photoresist process, interconnect widths are affected due to overlay error.



(a) **(b)**

Figure 4: Three interconnect layers shown. Side view. $P" \leq P \leq P'$ and $W" \leq W \leq W'$. (a) In a positive photoresist SDP process, interconnects printed after spacer formation may differ in width due to photoresist thickness variations S. (b) In a negative photoresist SDP process, interconnect widths and pitches are affected due to photoresist variations.

corners.[3] Once all simulations are conducted, minimum, nominal and maximum values for each coupling capacitance are recorded and the results are presented in the variational capacitance table.

3.2 Double Patterning Process

In this section, we describe the modifications needed for adapting the variational interconnect analysis for a double patterning process. With a double patterning process, mask shifts introduce an additional source of variability.

In Figure 2, we have already decomposed interconnects for mask1 and mask2 of a double patterning process. Interconnects with the number "1" and "2" on them will be printed using mask1 and mask2, respectively, whereas both would have been on the same mask in a traditional process.[4]

In Figure 3(a), we assume that the interconnects printed using mask2 are shifted by S due to overlay error in a positive photoresist DE or DP process.[5] S is assumed positive in the figure. A negative value would correspond to a shift in the opposite direction for edges of an interconnect. Notice that intralayer coupling increases on one side, whereas it reduces on the other side. We alter our DOE such that the mask shift parameter S is set equal to -3σ and 3σ conditions, with 1σ increments in between, in our variational corner analysis.

Figure 3(b) shows the impact of overlay error on a negative photoresist DE or DP process. Figures 4(a)-(b) show the printed interconnects for positive and negative photoresist SDP processes, respectively.

Figures 5(a)-(b) show mask decomposition for a small layout for DE/DP or SDP processes, respectively, for positive photoresist.

- In (a), original patterns 1-6 are split into two groups "Patterns 1" and "Patterns 2", and then printed in different lithography steps. Overlay error shifts "Patterns 2" by S and results in space variation in the final implemented patterns as shown in the fifth column.

- In (b), the second column depicts patterns 1, 4 and 5 which are assigned to the first lithography mask. Patterns 4 and 5 are assigned on the same line (second black box in the second column), and pattern 6 needs an additional dummy line (rightmost black box in the second column) printed to define the right edge of pattern 6. Thickness variations of spacers can result in narrower space between spacers as shown in the third column. Trim patterns in the fourth column are then used to remove unintentional surrounding patterns and to separate merged patterns a and b into original patterns 2 and 3, and 4 and 5. Finally, SDP may result in width variations ($W'' \leq W$).

For these process options, we alter the width and pitch of the structures as necessary to simulate mask shift-induced (translation) overlay error. Although it may be possible to reduce translational overlay error in the future, according to the ITRS it will not be possible to completely eliminate it from the process [1].

[3] The DOE can be simplified by eliminating certain corner combinations if they are known not to cause a worst-case corner based on a previous sensitivity analysis. However, the overall simulation time is already not burdensome.

[4] Notice that interconnects assigned to mask1 or mask2 have twice the pitch with respect to the final interconnect pitch. It is this pitch-doubling feature that helps double patterning achieve printability of finer-pitch interconnects than a traditional process.

[5] S is a parameter for which a 3σ value is provided by the lithography tool supplier for DE or DP processes; for the SDP process, S is the spacer thickness variation provided by the foundry.

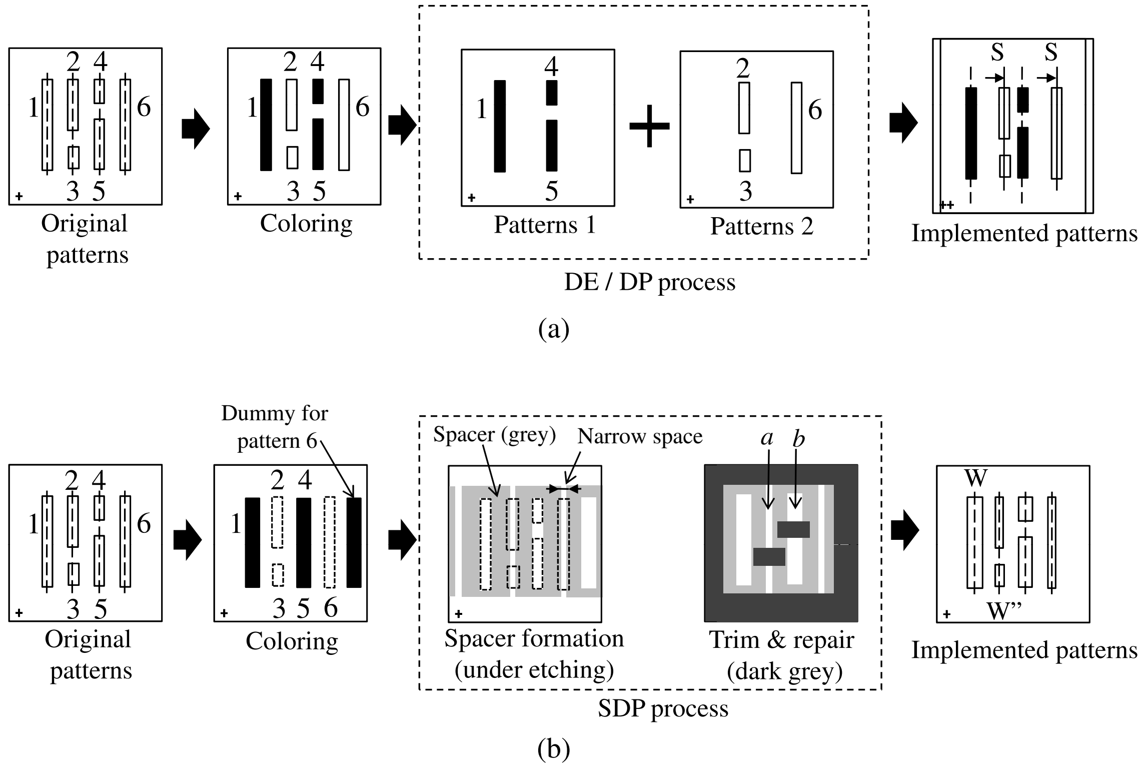


Figure 5: (a) A positive photoresist DE or DP process. (b) A positive photoresist SDP process. Dotted lines in the original and implemented patterns represent the target locations of the patterns. Dotted boxes in (b) are original patterns, overlaid on mask and spacer patterns for better understanding.

4. FULL-CHIP ANALYSIS

In this section, we discuss the full-chip design preparation and analysis.

4.1 Design Preparation Flow

In a traditional RC extraction flow, commercial tools directly read an entire design database, e.g., design exchange format (DEF), GDS, etc., and extract RC with given capacitance tables which contain width or height variation of metal or dielectric layers. However, to account for overlay error in double patterning process which is not included in the capacitance table, a new RC extraction flow that resembles the actual double patterning process is required.

From a routed layout of a full-chip design, we stream out GDS for all layers. We apply double patterning layer decomposition "*coloring*" to small pitch local interconnect layers, which may require double patterning. To decompose a layer into two masks, $layer_{mask1}$ and $layer_{mask2}$, we use the integer linear programming (ILP) based min-cost coloring assignment in [24]. We generate a base GDS that has all front end of line (FEOL) layers, i.e., nwell, active, p-implant, and the BEOL layers that do not use double patterning. For double patterning-applied layers, we generate two sub-GDS files per layer. Each sub-GDS contains only one double patterning mask obtained from the coloring step. To model overlay error, each double patterning mask layer in sub-GDS is shifted to a different origin point in the base GDS. For instance, to shift M2's first double patterning mask ($M2_{mask1}$) to the left by 10nm, the sub-GDS file that contains $M2_{mask1}$ is generated and located at (-10nm, 0nm) point in the base GDS file's coordinate system. For width variation, we use shape operators *OVERSIZE* and *UNDERSIZE* commands in *Synopsys Hercules(v2006.12-8)* to expand or shrink original patterns of specific layers.

Input: Mask $\in$ { $M2_{mask1}$ $M2_{mask2}$ $M3_{mask1}$ $M3_{mask2}$ $M4_{mask1}$ $M4_{mask2}$ $M5_{mask1}$ $M5_{mask2}$ };
Overlay error(S) $\in$ {3σ=10.4nm, 2σ=6.9nm, 1σ=3.5nm};
Width variation(ΔW) $\in$ {3σ=10.4nm, 2σ=6.9nm, 1σ=3.5nm}
Output: RC parasitic file (.SPEF) and timing reports

foreach *layer* $\in$ {M2, M3, M4, M5}
  foreach $S \in$ {-3σ/2, -2σ/2, -1σ/2, 0σ, 1σ/2, 2σ/2, 3σ/2}
    if *layer*'s preferred direction is *vertical*
      shift $layer_{mask1}$ left by S
      shift $layer_{mask2}$ right by S
    if *layer*'s preferred direction is *horizontal*
      shift $layer_{mask1}$ down by S
      shift $layer_{mask2}$ up by S
    merge layers
    foreach $W \in$ {-3σ, -2σ, -1σ, 0σ, 1σ, 2σ, 3σ}
      resize *layer* by ΔW
      RC parasitic extraction and timing analysis

Figure 6: Design of experiment (DOE) for full-chip analysis.

4.2 Analysis Flow

We permute all possible combinations of overlay error of each layer and width variation to measure the capacitance changes. From our preliminary studies, we observe that the interlayer coupling and via capacitance are not significant. So, we reduce the number of combinations by analyzing impact of each layer independent of other layers.

We assume six discrete overlay error locations and width variations, i.e., -3σ, -2σ, -1σ, 1σ, 2σ, and 3σ. We utilize direct align-

Table 2: Capacitance ($aF/\mu m$) results.

$aF/\mu m$	C^{down}_{min}	C^{down}_{nom}	C^{down}_{max}	C^{top}_{min}	C^{top}_{nom}	C^{top}_{max}	C^{intra}_{min}	C^{intra}_{nom}	C^{intra}_{max}	C^{total}_{min}	C^{total}_{nom}	C^{total}_{max}
Positive PR, *DA*, Overlay Variations Only	30.7	30.8	30.8	31.4	31.4	31.4	56.0	68.1	85.4	200	200	205
Positive PR, *DA*, Width Variations Only	30.1	30.8	31.2	30.9	31.4	31.8	55.7	68.1	85.7	174	200	222
Positive PR, *DA*, All Variations	25.3	30.8	38.8	25.8	31.4	39.7	36.1	68.1	135	152	200	283
Positive PR, *IA*, Overlay Variations Only	30.7	30.8	30.8	31.3	31.4	31.4	51.9	68.1	95.2	200	200	210
Positive PR, *IA*, Width Variations Only	30.1	30.8	31.2	30.9	31.4	31.8	55.7	68.1	85.7	174	200	222
Positive PR, *SDP*, Overlay Variations Only	29.4	30.8	30.8	30.0	31.4	31.4	61.4	68.1	76.0	189	200	200
Positive PR, *SDP*, All Variations	24.6	30.8	39.5	25.1	31.4	40.6	48.5	68.1	90.3	165	200	236
Negative PR, *DA*, Overlay Variations Only	27.4	30.8	33.0	28.1	31.4	33.7	67.9	68.1	68.1	192	200	204
Negative PR, *DA*, Height Variations Only	30.7	30.8	30.8	31.4	31.4	31.5	57.4	68.1	78.8	178	200	214
Negative PR, *DA*, All Variations	22.4	30.8	43.0	23.0	31.4	43.8	43.6	68.1	102	145	200	271
Negative PR, *IA*, Overlay Only	26.0	30.8	34.0	26.7	31.4	34.6	67.8	68.1	68.1	189	200	206
Negative PR, *IA*, Height Only	30.7	30.8	30.8	31.4	31.4	31.5	57.4	68.1	78.8	178	200	214
Negative PR, *SDP*, Overlay Variations Only	30.4	30.8	30.8	31.1	31.4	31.4	55.8	68.1	68.2	187	200	200
Negative PR, *SDP*, All Variations	25.6	30.8	38.4	26.1	31.4	39.3	43.9	68.1	99.1	163	200	242

Table 1: Technology stack parameters.

Layer	W_{nom}	H_{nom}	D_{nom}	$W_{3\sigma}$	$H_{3\sigma}$	$D_{3\sigma}$
poly	45nm	80nm	160nm	-	-	-
M1	52nm	94nm	94nm	-	-	-
M2	52nm	94nm	94nm	-	-	-
M3∼M5	68nm	122nm	122nm	13.6nm	24.4nm	24.4nm
M6, M7	104nm	188nm	188nm	-	-	-

ment due to small overlay error between double patterning masks. For worst cases in each layer, we assume that double patterning masks in a layer are shifted in opposite directions. We also assume that vertical layers are shifted in the horizontal direction and that horizontal layers are shifted in the vertical direction, since these shifts cause the largest changes in the distance between parallel lines.

The proposed DOE is summarized in Figure 6. With the output parasitic files (.SPEF), we analyze timing and capacitance variations for individual nets, timing-critical paths, and full-chip timing.

5. EXPERIMENTAL RESULTS

5.1 Interconnect Analysis Setup

We design a representative 45*nm* technology and, based on the International Technology Roadmap for Semiconductors [1], generate the interconnect nominal and 3σ dimensions given in Table 1. We use a 3σ value equal to 20% of nominal interconnect dimensions both for interconnect variations as well as the mask shift parameter *S* for a fair comparison between interconnect variations and overlay error. We use an effective dielectric constant of 3.3 all around the interconnects.

5.2 Interconnect Analysis Results

We conduct our experiments with positive vs. negative photoresists, as well as direct vs. indirect alignment to be able to compare these options in terms of capacitive effects. We provide the results in Table 2.

In Table 2, overlay only indicates that the only variation source is overlay error. Similarly, in different rows, we turn on width only, height only, or all variation sources. C^{down}, C^{top}, and C^{intra} are the capacitances to the lower, upper, and intralayer interconnects, respectively. C^{total} is the total capacitance. Subscripts *min*, *nom*, and *max* indicate minimum, nominal and maximum cases, respectively. If it is not an SDP process, the results can be used for either DE or DP processes. We observe that directly aligned (*DA*) positive PR results in similar capacitive impact due to overlay error or width variations. Indirect aligned (*IA*) cases result in higher capacitance changes as compared to *DA* cases with respect to nominal for the positive PR case.

Intralayer coupling capacitance correlates quite well to noise or coupling-induced delay at the circuit level. Total capacitances, on the other hand, correlate well with circuit delay. In the next section, we present our full-chip analysis results for the positive photoresist DE or DP case for direct alignment.

5.3 Full-Chip Analysis Setup

For the BEOL stack, we use five '1x' layers, i.e., M1, M2, M3, M4 and M5, and two '2x' layers, i.e., M6 and M7. 1x layers have roughly half width and thickness of 2x layers, and M1 and M2 have smaller design rules than other 1x layers as shown in Table 1. We assume double patterning is applied to 1x layers, and then we apply the new RC extraction methodology in Section IV-A. We assume 20% of M1 design rules as 3σ variation of overlay error and width, i.e., 10.4nm for each.[6]

We implement the *AES* core, obtained as RTL from the open-source site *opencores.org* [26]. With 4ns clock cycle time, we perform synthesis, placement and routing with NanGate 45nm Open-Library [25] using *Cadence RTL Compiler v5.2* [30] and *Cadence SOC Encounter v7.2* [32]. Finally, 26,069 instances (standard cells) are placed with 86% utilization and routed with average 10% (maximum 14%) metal density.[7] We extract GDS from the routed design and apply double patterning coloring to M1 to M5 layers. To shift and merge GDS files, we implement SKILL command scripts with *Cadence Virtuoso Layout Design Environment IC6.1.0.243* [31]. We use *Synopsys STAR-RCXT v2007.06* [27] for RC extraction and *Synopsys PrimeTime-SI vB-2008.12-SP2* [29] for static timing analysis.

5.4 Full-Chip Analysis Results

Table 3 shows crosstalk-induced delay changes of a net which has the largest crosstalk-induced delay in the *AES* testcase. This net consists of three interconnect segments; 1.604um M2, 0.78um M3 and 14.788um M4. M2 segment has one neighbor net with minimum space on one side of the segment, M3 segment does not have a neighbor net within minimum distance. Each side of M4 segment is fully filled with neighbor nets with minimum distance. As we expect, overlay error and width variation of M3 and M5 layers shows small impact (less than 3%) on crosstalk-induced delay, since interlayer coupling is relatively small and there is no intralayer coupling. M2 overlay error to -3σ that leads to smaller space between M2 segment and its neighbor results to maximum 13% increase of crosstalk-induced delay, and M2 +3σ width increase that also leads to smaller space with a neighbor net shows maximum 16% of crosstalk-induced delay. Unlike the two parallel line case of M2 segment, M4 width variation affects maximum 23% which comes from the coupling increase of both sides, but M4 overlay error has

[6]Impact of M1 coloring and overlay error are included in cell characterization, so M1 can be excluded in circuit level DOE.

[7]Metal density is calculated from only signal nets. Maximum value is 50% when all routing tracks are used. Including power and ground network will increase metal density.

small impact on crosstalk-induced delay, since coupling of one side decreases when that of the other side increases in the three parallel line structure. These results are well matched to the conclusion of [23].

Table 3: Maximum crosstalk-induced delay variation with respect to overlay error in row indices and width variation in column indices for each double patterning-applied layer. 0σ for width and overlay error corresponds to the nominal case.

Overlay error	ΔW						
($Mask_1$, $Mask_2$)	-3σ	-2σ	-1σ	0σ	1σ	2σ	3σ
M2	Maximum Δdelay(ns)						
(-3σ/2, 3σ/2)	0.296	0.298	0.338	0.339	0.344	0.345	0.346
(-2σ/2, 2σ/2)	0.300	0.297	0.299	0.338	0.348	0.346	0.349
(-1σ/2, 1σ/2)	0.300	0.295	0.298	0.339	0.342	0.345	0.348
(0σ, 0σ)	0.300	0.299	0.297	0.300	0.341	0.342	0.346
(1σ/2, -1σ/2)	0.299	0.296	0.300	0.299	0.339	0.339	0.345
(2σ/2, -2σ/2)	0.300	0.299	0.297	0.299	0.298	0.339	0.344
(3σ/2, -3σ/2)	0.298	0.296	0.300	0.299	0.301	0.337	0.343
M3	Maximum Δdelay(ns)						
(-3σ/2, 3σ/2)	0.306	0.307	0.307	0.302	0.301	0.297	0.299
(-2σ/2, 2σ/2)	0.304	0.307	0.302	0.303	0.299	0.300	0.298
(-1σ/2, 1σ/2)	0.306	0.306	0.302	0.303	0.300	0.300	0.299
(0σ, 0σ)	0.307	0.344	0.305	0.300	0.299	0.301	0.300
(1σ/2, -1σ/2)	0.309	0.304	0.304	0.300	0.302	0.300	0.300
(2σ/2, -2σ/2)	0.305	0.304	0.304	0.300	0.300	0.300	0.299
(3σ/2, -3σ/2)	0.303	0.306	0.302	0.303	0.302	0.299	0.301
M4	Maximum Δdelay(ns)						
(-3σ/2, 3σ/2)	0.275	0.294	0.315	0.304	0.332	0.330	0.361
(-2σ/2, 2σ/2)	0.274	0.292	0.319	0.304	0.330	0.356	0.365
(-1σ/2, 1σ/2)	0.275	0.289	0.315	0.304	0.331	0.355	0.367
(0σ, 0σ)	0.275	0.287	0.312	0.300	0.330	0.356	0.368
(1σ/2, -1σ/2)	0.270	0.292	0.313	0.298	0.327	0.354	0.365
(2σ/2, -2σ/2)	0.272	0.293	0.314	0.300	0.327	0.351	0.366
(3σ/2, -3σ/2)	0.276	0.292	0.316	0.300	0.324	0.344	0.360
M5	Maximum Δdelay(ns)						
(-3σ/2, 3σ/2)	0.304	0.303	0.302	0.299	0.299	0.299	0.299
(-2σ/2, 2σ/2)	0.302	0.302	0.302	0.301	0.300	0.299	0.301
(-1σ/2, 1σ/2)	0.303	0.303	0.301	0.301	0.300	0.299	0.298
(0σ, 0σ)	0.304	0.302	0.301	0.300	0.300	0.300	0.297
(1σ/2, -1σ/2)	0.305	0.304	0.304	0.299	0.301	0.299	0.300
(2σ/2, -2σ/2)	0.303	0.303	0.302	0.301	0.299	0.298	0.296
(3σ/2, -3σ/2)	0.305	0.305	0.302	0.300	0.300	0.298	0.300

Table 4 distinguishes coupling capacitance and ground capacitance of the net used for Table 3. We observe coupling capacitance of this net is about 2x larger than ground capacitance, which is a reason of the large crosstalk-induced delay changes.

Table 5 shows, interconnect capacitance changes of the top 4,888 high capacitance nets (≥1fF) in *AES*. Each tuple in the table entries shows maximum capacitance increase, maximum capacitance decrease and average capacitance change respectively. We observe maximum 28.6% from +3σ width variation of M2 and 9.7% capacitance changes from 3σ overlay error (mask1 moves 3σ/2 and mask2 moves -3σ/2) of M2. We note that average changes are quite small, since capacitance increase of a set of nets compensates capacitance decrease of the other set of nets. However, the large increase and decrease of capacitance at one corner result in larger on-chip variations in timing analysis.

Table 6 shows maximum delay changes among all timing violated paths in the design from overlay error and width variation. Impact of overlay error is negligibly small (∼1%), but width variation can change the path delay by 3.6%. These results can be explained by Table 5 which shows maximum 4.8% capacitance changes on average among all DOE simulations.

Table 7 shows total negative slack (TNS) changes from overlay error and width variation. Compared with results of the path delay changes in Table 6, TNS shows accumulated impact on most timing critical nets, so TNS can change up to 49% due to width variation and up to 4% due to overlay error.

From the design-level experimental results, we observe that both overlay error and width variation have similar impact on coupling-induced delay. Coupling-induced delay due to overlay error is more than 10%.

6. CONCLUSIONS

We have provided a variational interconnect analysis technique for double patterning lithography processes. We have compared interconnect variations with overlay error-based variations in DPL technologies. We have applied our technique on a 45*nm* process at both interconnect and full-chip circuit levels. We have seen that for the given process, overlay errors do not significantly change coupling capacitances to upper and lower layers.

Whether overlay error is more important than CD control depends on the choice of double patterning technology. We believe that our study framework can help target overlay error metrics from a performance-based point of view. We provide the following conclusions.

1. In double exposure (DE) and double patterning (DP) techniques, indirect alignment (IA) results in higher capacitance variation with overlay error than direct alignment (DA).
2. Thickness control in spacer double patterning can be relaxed as compared to overlay error control in DE or DP techniques.
3. Overlay error can cause up to 10% capacitance variation and up to 13% increase of coupling-induced delay variation.
4. Total negative slack is more sensitive to width variation than to overlay error.

Our future work entails full-chip evaluation of SDP, metal fill impacts, FEOL impacts, coupling-induced delay and noise, as well as incorporation of secondary overlay components in DPL methodologies.

7. ACKNOWLEDGMENTS

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Table 4: Coupling and ground capacitance changes of a net having maximum crosstalk-induced delay variation with respect to overlay error in row indices and width variation in column indices for each double patterning-applied layer. 0σ for width and overlay error corresponds to the nominal reference case.

Overlay error	ΔW						
($Mask_1$, $Mask_2$)	-3σ	-2σ	-1σ	0σ	1σ	2σ	3σ
M2	Coupling capacitance(fF),Ground capacitance(fF)						
(-3σ/2, 3σ/2)	1.829, 1.079	1.839, 1.049	1.865, 1.046	1.876, 1.077	1.895, 1.124	1.903, 1.156	1.905, 1.137
(-2σ/2, 2σ/2)	1.833, 1.053	1.834, 1.088	1.849, 1.058	1.869, 1.062	1.906, 1.053	1.904, 1.134	1.910, 1.087
(-1σ/2, 1σ/2)	1.836, 1.045	1.828, 1.112	1.844, 1.087	1.863, 1.053	1.882, 1.093	1.899, 1.140	1.911, 1.094
(0σ, 0σ)	1.822, 1.034	1.834, 1.050	1.840, 1.089	1.859, 1.087	1.882, 1.079	1.894, 1.173	1.906, 1.120
(1σ/2, -1σ/2)	1.811, 1.034	1.820, 1.131	1.838, 1.082	1.842, 1.089	1.867, 1.071	1.874, 1.117	1.900, 1.119
(2σ/2, -2σ/2)	1.813, 1.050	1.820, 1.070	1.826, 1.080	1.848, 1.085	1.861, 1.139	1.876, 1.139	1.896, 1.124
(3σ/2, -3σ/2)	1.806, 1.057	1.810, 1.116	1.827, 1.087	1.837, 1.067	1.855, 1.096	1.861, 1.101	1.890, 1.112
M3	Coupling capacitance(fF), Ground capacitance(fF)						
(-3σ/2, 3σ/2)	1.883, 1.064	1.883, 1.040	1.887, 1.071	1.864, 1.073	1.857, 1.105	1.850, 1.160	1.858, 1.126
(-2σ/2, 2σ/2)	1.882, 1.066	1.879, 1.022	1.861, 1.063	1.863, 1.076	1.855, 1.122	1.868, 1.150	1.843, 1.130
(-1σ/2, 1σ/2)	1.887, 1.073	1.880, 1.045	1.857, 1.075	1.870, 1.096	1.855, 1.107	1.858, 1.137	1.852, 1.121
(0σ, 0σ)	1.880, 1.054	1.888, 1.049	1.870, 1.029	1.859, 1.087	1.856, 1.150	1.860, 1.122	1.854, 1.146
(1σ/2, -1σ/2)	1.893, 1.036	1.866, 1.067	1.865, 1.063	1.852, 1.088	1.857, 1.069	1.864, 1.163	1.857, 1.143
(2σ/2, -2σ/2)	1.877, 1.060	1.861, 1.064	1.875, 1.083	1.858, 1.064	1.853, 1.113	1.859, 1.115	1.853, 1.127
(3σ/2, -3σ/2)	1.869, 1.072	1.889, 1.070	1.863, 1.109	1.859, 1.054	1.860, 1.086	1.856, 1.153	1.863, 1.148
M4	Coupling capacitance(fF), Ground capacitance(fF)						
(-3σ/2, 3σ/2)	1.486, 1.037	1.588, 1.046	1.724, 1.100	1.869, 1.091	2.021, 1.059	2.117, 1.083	2.211, 1.057
(-2σ/2, 2σ/2)	1.484, 1.019	1.591, 1.052	1.730, 1.048	1.859, 1.079	2.035, 1.138	2.196, 1.095	2.259, 1.070
(-1σ/2, 1σ/2)	1.483, 1.001	1.572, 1.047	1.713, 1.042	1.876, 1.101	2.040, 1.142	2.191, 1.061	2.263, 1.074
(0σ, 0σ)	1.493, 0.972	1.586, 1.117	1.714, 1.098	1.859, 1.087	2.035, 1.050	2.225, 1.158	2.262, 1.028
(1σ/2, -1σ/2)	1.475, 1.042	1.578, 1.028	1.715, 1.061	1.856, 1.101	2.039, 1.110	2.204, 1.124	2.262, 1.078
(2σ/2, -2σ/2)	1.487, 1.041	1.598, 1.019	1.721, 1.013	1.868, 1.050	2.042, 1.104	2.191, 1.075	2.264, 1.106
(3σ/2, -3σ/2)	1.501, 0.983	1.596, 0.995	1.729, 1.026	1.876, 1.072	2.030, 1.081	2.149, 1.092	2.236, 1.104
M5	Coupling capacitance(fF), Ground capacitance(fF)						
(-3σ/2, 3σ/2)	1.876, 1.064	1.877, 1.119	1.867, 1.074	1.864, 1.130	1.857, 1.119	1.866, 1.148	1.857, 1.132
(-2σ/2, 2σ/2)	1.878, 1.101	1.871, 1.098	1.868, 1.085	1.862, 1.059	1.864, 1.124	1.859, 1.124	1.863, 1.094
(-1σ/2, 1σ/2)	1.874, 1.077	1.879, 1.097	1.866, 1.094	1.869, 1.131	1.864, 1.113	1.857, 1.135	1.853, 1.105
(0σ, 0σ)	1.879, 1.054	1.873, 1.088	1.866, 1.118	1.859, 1.087	1.859, 1.090	1.864, 1.107	1.855, 1.152
(1σ/2, -1σ/2)	1.884, 1.079	1.881, 1.103	1.876, 1.090	1.862, 1.130	1.856, 1.073	1.860, 1.135	1.864, 1.126
(2σ/2, -2σ/2)	1.869, 1.078	1.878, 1.119	1.871, 1.100	1.859, 1.072	1.860, 1.121	1.854, 1.129	1.854, 1.160
(3σ/2, -3σ/2)	1.884, 1.097	1.883, 1.080	1.871, 1.100	1.869, 1.140	1.861, 1.096	1.858, 1.153	1.862, 1.113

Table 5: Interconnect capacitance changes of top 4,888 (20% of total net count) high interconnect capacitance nets with respect to overlay error in row indices and ΔW variation in column indices for each double patterning-applied layer. 0σ for width and overlay error corresponds to the nominal reference case.

Overlay error	ΔW						
($Mask_1$, $Mask_2$)	-3σ	-2σ	-1σ	0σ	1σ	2σ	3σ
M2	Capacitance changes(%): Maximum increase, Maximum decrease, Average changes						
(-3σ/2, 3σ/2)	6.6, -22.0, 4.6	4.9, -16.7, 3.4	5.3, -12.9, 2.0	9.2, -7.7, 1.4	16.3, -8.9, 2.3	24.6, -7.0, 3.6	28.0, -7.5, 5.0
(-2σ/2, 2σ/2)	6.3, -22.1, 4.6	5.5, -17.1, 3.4	6.7, -11.7, 2.1	8.2, -8.2, 1.3	18.8, -6.5, 2.3	21.3, -6.5, 3.8	27.9, -5.0, 5.3
(-1σ/2, 1σ/2)	6.6, -22.1, 4.7	6.3, -16.2, 3.5	6.2, -10.9, 2.1	8.7, -6.1, 1.3	15.4, -5.7, 2.3	23.3, -6.5, 4.0	26.9, -6.3, 5.3
(0σ, 0σ)	7.1, -22.2, 4.7	5.0, -16.6, 3.4	9.0, -10.8, 2.1	0.0, 0.0, 0.0	13.7, -5.7, 2.3	24.3, -5.4, 4.2	28.6, -3.6, 5.3
(1σ/2, -1σ/2)	5.7, -21.5, 4.7	5.6, -16.4, 3.5	7.3, -10.2, 2.1	8.1, -8.3, 1.3	15.1, -7.8, 2.3	23.0, -6.1, 3.9	27.9, -6.5, 5.3
(2σ/2, -2σ/2)	6.0, -21.4, 4.6	5.5, -17.1, 3.5	6.1, -11.3, 2.1	8.5, -8.6, 1.3	15.8, -6.0, 2.4	21.6, -5.9, 3.8	27.7, -5.2, 5.3
(3σ/2, -3σ/2)	9.2, -20.5, 4.5	7.7, -16.8, 3.4	6.1, -11.5, 2.0	9.7, -7.3, 1.4	15.3, -5.7, 2.3	20.4, -6.4, 3.6	24.2, -5.9, 5.0
M3	Capacitance changes(%): Maximum increase, Maximum decrease, Average changes						
(-3σ/2, 3σ/2)	6.8, -11.5, 2.3	6.3, -10.6, 1.8	7.5, -8.0, 1.5	8.5, -7.3, 1.3	12.9, -7.6, 1.5	17.8, -5.5, 1.9	15.4, -6.0, 2.4
(-2σ/2, 2σ/2)	5.9, -13.0, 2.3	6.4, -10.6, 1.9	8.3, -9.7, 1.5	7.5, -9.7, 1.4	9.9, -7.8, 1.5	11.3, -6.7, 1.9	15.0, -5.7, 2.3
(-1σ/2, 1σ/2)	11.3, -14.6, 2.3	8.0, -11.3, 1.9	8.9, -9.1, 1.5	9.1, -7.9, 1.3	10.6, -7.0, 1.5	11.4, -6.7, 1.9	17.7, -6.5, 2.4
(0σ, 0σ)	4.9, -13.8, 2.3	6.8, -11.0, 1.9	7.2, -8.8, 1.5	0.0, 0.0, 0.0	10.2, -7.2, 1.5	15.4, -5.5, 1.8	14.5, -6.5, 2.4
(1σ/2, -1σ/2)	7.2, -13.3, 2.3	6.7, -11.7, 1.9	7.6, -10.7, 1.5	7.9, -7.9, 1.3	9.1, -7.0, 1.5	10.9, -7.5, 1.9	13.8, -7.6, 2.4
(2σ/2, -2σ/2)	5.4, -12.6, 2.3	6.7, -10.1, 1.9	7.1, -9.5, 1.5	8.3, -7.4, 1.3	11.9, -6.6, 1.5	12.2, -7.1, 1.9	13.5, -5.9, 2.4
(3σ/2, -3σ/2)	7.0, -14.0, 2.3	7.0, -10.9, 1.9	7.9, -8.6, 1.5	9.6, -7.0, 1.3	9.8, -6.6, 1.5	11.3, -6.0, 1.9	14.7, -5.1, 2.3
M4	Capacitance changes(%): Maximum increase, Maximum decrease, Average changes						
(-3σ/2, 3σ/2)	5.5, -18.5, 4.8	5.9, -14.8, 3.5	6.6, -9.6, 2.1	8.5, -8.8, 1.4	13.2, -6.1, 2.3	14.4, -7.4, 3.3	18.3, -6.9, 4.6
(-2σ/2, 2σ/2)	6.9, -16.7, 4.8	6.9, -13.5, 3.5	7.5, -9.5, 2.2	8.2, -7.6, 1.4	10.9, -5.8, 2.3	16.2, -6.2, 3.6	17.6, -6.5, 4.9
(-1σ/2, 1σ/2)	7.0, -17.2, 4.8	7.3, -12.7, 3.5	7.0, -9.9, 2.1	9.3, -7.2, 1.3	10.8, -6.5, 2.2	16.3, -6.2, 3.7	17.8, -6.1, 4.8
(0σ, 0σ)	5.5, -17.1, 4.8	7.5, -13.0, 3.5	7.5, -9.8, 2.2	0.0, 0.0, 0.0	10.2, -6.5, 2.2	16.7, -6.8, 3.9	19.2, -6.0, 4.8
(1σ/2, -1σ/2)	5.9, -17.1, 4.8	7.4, -12.9, 3.5	8.0, -10.1, 2.1	8.7, -7.7, 1.3	10.5, -8.0, 2.2	16.5, -5.9, 3.7	18.1, -6.7, 4.9
(2σ/2, -2σ/2)	6.5, -18.3, 4.8	7.6, -12.8, 3.5	8.0, -9.4, 2.1	8.0, -8.9, 1.3	13.1, -9.1, 2.2	15.8, -6.9, 3.5	18.3, -7.2, 4.9
(3σ/2, -3σ/2)	7.2, -17.9, 4.7	5.4, -14.1, 3.5	7.5, -10.0, 2.1	9.3, -8.2, 1.4	11.1, -9.1, 2.2	13.4, -6.7, 3.3	17.2, -6.3, 4.6
M5	Capacitance changes(%): Maximum increase, Maximum decrease, Average changes						
(-3σ/2, 3σ/2)	6.7, -12.9, 2.3	8.7, -11.0, 1.9	8.6, -9.8, 1.5	7.5, -8.2, 1.3	10.3, -6.8, 1.5	12.2, -6.6, 1.9	17.1, -5.8, 2.5
(-2σ/2, 2σ/2)	6.5, -12.3, 2.4	7.2, -11.5, 1.9	7.7, -8.1, 1.5	8.5, -6.7, 1.3	9.1, -6.0, 1.5	12.2, -6.6, 1.9	16.7, -7.0, 2.4
(-1σ/2, 1σ/2)	6.5, -12.7, 2.4	8.4, -10.5, 1.9	7.6, -8.6, 1.5	7.1, -7.2, 1.2	10.3, -6.2, 1.5	14.2, -6.6, 1.9	16.7, -7.2, 2.5
(0σ, 0σ)	8.1, -12.8, 2.4	7.6, -11.0, 1.9	8.8, -9.2, 1.5	0.0, 0.0, 0.0	10.2, -7.0, 1.5	11.7, -6.9, 1.9	14.8, -6.7, 2.4
(1σ/2, -1σ/2)	8.0, -13.1, 2.4	7.5, -11.9, 1.9	10.4, -10.0, 1.5	6.6, -8.6, 1.2	9.7, -7.0, 1.5	12.2, -7.2, 1.9	16.8, -6.4, 2.4
(2σ/2, -2σ/2)	6.3, -11.9, 2.4	7.1, -12.1, 1.9	8.4, -8.0, 1.5	7.7, -7.2, 1.3	9.0, -5.7, 1.4	12.1, -8.3, 1.9	14.5, -6.5, 2.5
(3σ/2, -3σ/2)	7.4, -11.7, 2.4	9.0, -10.5, 1.9	6.4, -9.0, 1.5	9.1, -8.7, 1.3	9.6, -7.0, 1.5	12.7, -6.1, 1.9	17.8, -6.4, 2.5

Table 6: Maximum delay variation among all violated paths with respect to overlay error in row indices and ΔW variation in column indices for each double patterning-applied layer. 0σ for width and overlay error corresponds to the nominal case.

Overlay error	ΔW						
($Mask_1$, $Mask_2$)	-3σ	-2σ	-1σ	0σ	1σ	2σ	3σ
M2	Maximum path delay variation (%)						
(-3σ/2, 3σ/2)	3.093	2.192	1.442	0.984	1.682	2.316	3.109
(-2σ/2, 2σ/2)	3.154	2.304	1.027	0.949	1.747	2.281	3.724
(-1σ/2, 1σ/2)	3.113	2.522	1.357	0.946	1.597	2.511	3.560
(0σ, 0σ)	3.077	2.292	1.570	0.000	1.771	2.807	3.270
(1σ/2, -1σ/2)	2.657	2.115	1.475	0.702	1.577	2.809	3.655
(2σ/2, -2σ/2)	2.952	2.309	1.416	0.807	1.847	2.626	3.627
(3σ/2, -3σ/2)	2.913	1.866	1.392	1.231	1.973	2.744	3.243
M3	Maximum path delay variation (%)						
(-3σ/2, 3σ/2)	1.233	0.833	0.672	0.642	0.737	0.846	1.213
(-2σ/2, 2σ/2)	1.192	0.939	0.672	0.475	0.896	0.901	1.024
(-1σ/2, 1σ/2)	1.075	0.917	0.613	0.487	0.775	1.089	1.180
(0σ, 0σ)	1.170	0.832	0.719	0.000	0.833	0.880	1.395
(1σ/2, -1σ/2)	1.237	0.891	0.575	0.720	0.760	0.900	1.257
(2σ/2, -2σ/2)	0.954	0.855	0.576	0.567	0.531	0.956	1.108
(3σ/2, -3σ/2)	1.153	0.843	0.683	0.510	0.612	1.379	1.298
M4	Maximum path delay variation (%)						
(-3σ/2, 3σ/2)	2.705	2.147	1.804	1.053	1.604	1.959	3.177
(-2σ/2, 2σ/2)	2.616	2.060	1.809	0.993	1.682	2.492	3.329
(-1σ/2, 1σ/2)	2.546	1.971	1.876	0.969	1.504	2.423	3.190
(0σ, 0σ)	3.137	2.472	1.217	0.000	1.484	2.784	3.507
(1σ/2, -1σ/2)	2.911	2.514	1.008	0.600	1.470	2.594	3.639
(2σ/2, -2σ/2)	3.021	2.229	1.607	0.644	1.585	2.440	3.363
(3σ/2, -3σ/2)	2.953	2.475	1.653	0.777	1.428	2.101	3.586
M5	Maximum path delay variation (%)						
(-3σ/2, 3σ/2)	0.820	0.702	0.499	0.665	0.572	0.900	1.129
(-2σ/2, 2σ/2)	0.820	0.810	0.635	0.429	0.651	0.852	1.129
(-1σ/2, 1σ/2)	0.870	0.745	0.662	0.669	0.511	0.734	0.948
(0σ, 0σ)	0.892	0.750	0.615	0.000	0.671	0.961	1.054
(1σ/2, -1σ/2)	0.842	0.707	0.588	0.639	0.752	0.801	1.170
(2σ/2, -2σ/2)	0.861	0.747	0.620	0.520	0.812	0.839	1.032
(3σ/2, -3σ/2)	0.739	0.643	0.765	0.615	0.708	0.706	1.035

Table 7: Total negative slack (TNS) variation with respect to overlay error in row indices and ΔW variation in column indices for each double patterning-applied layer. 0σ for width and overlay error corresponds to the nominal reference case.

Overlay error	ΔW						
($Mask_1$,$Mask_2$)	-3σ	-2σ	-1σ	0σ	1σ	2σ	3σ
M2	TNS variation (ns)						
(-3σ/2, 3σ/2)	-24.0	-27.0	-32.2	-37.3	-43.1	-47.3	-52.5
(-2σ/2, 2σ/2)	-23.6	-26.8	-31.5	-36.6	-43.2	-48.8	-53.6
(-1σ/2, 1σ/2)	-23.8	-26.6	-31.3	-36.4	-42.9	-49.3	-53.9
(0σ, 0σ)	-23.6	-26.5	-31.7	-35.9	-43.0	-50.4	-53.6
(1σ/2, -1σ/2)	-23.7	-26.9	-31.5	-36.0	-43.1	-49.4	-53.8
(2σ/2, -2σ/2)	-23.7	-26.9	-31.4	-36.4	-42.8	-48.6	-53.6
(3σ/2, -3σ/2)	-24.4	-27.0	-31.4	-37.0	-42.7	-47.9	-52.2
M3	TNS variation (ns)						
(-3σ/2, 3σ/2)	-32.9	-33.5	-35.1	-36.2	-37.0	-38.1	-39.7
(-2σ/2, 2σ/2)	-32.8	-33.6	-35.1	-36.0	-37.1	-38.2	-39.4
(-1σ/2, 1σ/2)	-32.4	-33.7	-35.0	-36.0	-37.0	-38.3	-39.3
(0σ, 0σ)	-32.6	-33.9	-34.7	-35.9	-37.3	-38.3	-39.6
(1σ/2, -1σ/2)	-32.6	-33.7	-35.0	-35.8	-37.0	-38.3	-39.3
(2σ/2, -2σ/2)	-32.9	-33.8	-35.1	-35.7	-36.7	-38.2	-39.2
(3σ/2, -3σ/2)	-32.9	-33.8	-34.6	-36.0	-36.7	-38.2	-39.3
M4	TNS variation (ns)						
(-3σ/2, 3σ/2)	-26.8	-29.4	-32.5	-36.0	-40.3	-43.3	-47.2
(-2σ/2, 2σ/2)	-26.9	-29.4	-32.4	-35.8	-40.4	-44.2	-48.4
(-1σ/2, 1σ/2)	-26.8	-29.4	-32.3	-36.1	-40.5	-44.7	-48.3
(0σ, 0σ)	-26.7	-29.2	-32.3	-35.9	-40.7	-45.7	-48.0
(1σ/2, -1σ/2)	-26.5	-29.1	-32.8	-36.3	-40.5	-45.4	-48.3
(2σ/2, -2σ/2)	-26.8	-29.2	-32.6	-36.2	-40.7	-44.4	-48.0
(3σ/2, -3σ/2)	-26.7	-29.2	-33.0	-36.4	-40.7	-43.9	-47.4
M5	TNS variation (ns)						
(-3σ/2, 3σ/2)	-33.4	-34.3	-34.8	-35.9	-36.8	-38.1	-39.1
(-2σ/2, 2σ/2)	-33.2	-34.1	-34.9	-35.9	-36.7	-37.7	-38.8
(-1σ/2, 1σ/2)	-33.6	-34.1	-35.2	-36.0	-36.8	-37.9	-38.8
(0σ, 0σ)	-33.2	-34.1	-35.2	-35.9	-36.7	-37.9	-39.0
(1σ/2, -1σ/2)	-33.2	-34.0	-35.0	-36.0	-36.9	-38.0	-39.2
(2σ/2, -2σ/2)	-33.3	-33.9	-34.9	-35.9	-36.8	-37.9	-39.2
(3σ/2, -3σ/2)	-33.5	-33.9	-35.1	-36.0	-36.9	-37.8	-39.2

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