Closing the Loop in Interconnect Analyses and Optimization: CMP Fill, Lithography and Timing

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Abstract

In leading-edge chip designs, the dimensional variation that arises from lithography, etch, and planarization processes of multilevel metallization is significant due to its direct impact on wire parasitics and circuit timing. Modeling the dimensional variation helps reduce uncertainty in the extraction of parasitics and enables closure - not only of design, but of various process-design tradeoffs. Today, interconnect analyses and manufacturing are complicated by several close interactions among various components of the design and manufacturing flows. Our research program explores many of these previously-ignored, cross-domain interactions for multilevel interconnect, including those between lithography, topography, dummy fill, and circuit performance. Studies described in this paper include wire CD control through topography-aware OPC; accurate parasitic extraction by modeling wire sidewall angle and dummy fill; and timing-driven, intelligent CMP fill synthesis.

I. Introduction

Analyses, optimization and manufacturing of multilevel interconnect have become extremely challenging with the scaling of process geometries. In sub-100nm technologies, it is no longer acceptable to ignore interactions between various components of the interconnect design-to-manufacturing flow. Parasitic extraction, CMP fill, topography and lithography are unquestionably among the components whose interactions require explicit modeling.

In the past decade, chemical-mechanical planarization (CMP) has emerged as the predominant planarization technique for multilevel metallization. However, significant surface topography variation can still exist for some layout patterns; this impacts depth of focus in lithography. Presently, optical proximity correction (OPC) methods are oblivious to the predictable nature of focus variation, leading to a loss of wire width control. At the same time OPC methods are not able to perfectly correct lithographic and etch deviations, especially with varying process conditions. In this context, it becomes important to estimate interconnect parasitics taking into account wire width and wire sidewall angle deviations.

To help meet stringent topography requirements in today's advanced technologies, CMP fill is inserted into the layout to make feature density distributions more uniform. The CMP fill is governed by CMP design rules which specify density bounds, sizes and spacing of dummies, spacing of dummies to wires, etc. Fill is often implemented by physical verification tools that find unoccupied spaces and simply insert dummy shapes into those areas. Often, the fill synthesis is performed in multiple passes, each with varying dummy sizes, with the explicit goal of maximizing the amount of fill inserted. Hence, CMP fill insertion can significantly affect interconnect capacitance, delay, and circuit performance. Improved modeling of fill impact on interconnect parasitics must be complemented by new "intelligent", performance-driven fill synthesis capabilities.

Our paper is organized as follows. In Section II, we discuss two example issues - post-CMP wafer topography and lithographic defocus, and performance analysis based on shapes obtained from lithography simulation - that pertain to the lithography process for interconnect. In Section III, we examine one prominent example of manufacturing non-ideality - sidewall angle - and its impact on interconnect performance.

Section IV discusses CMP fill and its impact on interconnect performance; we also sketch a strategy for intelligent fill synthesis. We conclude in Section V.

II. Lithographic Considerations for Interconnect

In this section, we discuss two example issues that pertain to the lithography process for interconnect: (1) defocus due to wafer topography, and (2) the closure of performance analysis with respect to deviations between drawn and printed interconnect shapes.

A. Topography-Aware Optical Proximity Correction

As optical lithography advances into the 90nm technology node and beyond, minimum feature size outpaces the introduction of advanced lithography hardware solutions. In particular, the minimum depth of focus margin required for manufacturability of metal layers is extremely difficult to achieve due to non-planar wafer topography. A root problem is that predictable and systematic variation in depth of focus is not modeled or exploited during the application of advanced reticle enhancement techniques such as optical proximity correction (OPC) and subresolution assist feature (SRAF) insertion. We motivate our work on TOPC (Topography-aware Optical Proximity Correction) with Figure 1(a), which shows how post-CMP thickness in copper-oxide polishing will *predictably* change with the region pattern density. The depth-of focus (DOF) variation corresponding to the thickness variation affects metal patterning of the subsequent upper layer, as shown in Figure 1(b) (results obtained using SOLID-C lithography simulation from Sigma-C). Our new TOPC methodology informs OPC insertion by estimated defocus values derived from CMP

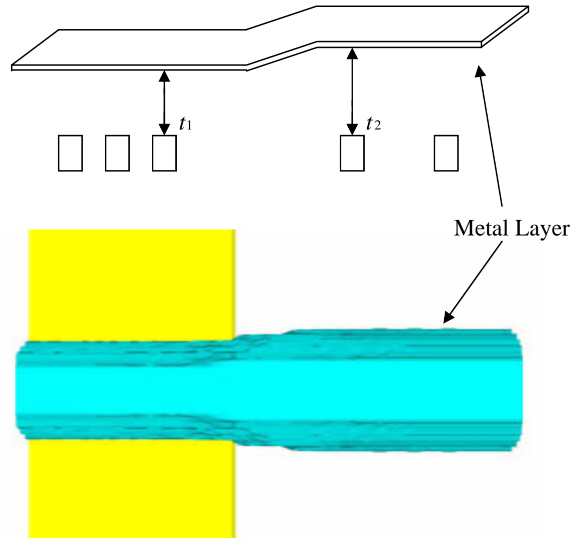

Fig. 1. (a) Side view showing thickness variation over regions with dense and sparse layout. (b) Top view showing CD variation when a line is patterned over a region with uneven wafer topography, i.e., under conditions of varying defocus.

simulation. After fabrication of a given chip layer, variation in topography creates focus variation in the lithography used to create the next layer of chip. We use CMP simulation to compute a topographic map over the chip layout; this yields for each layout feature an associated height $h(f_i)$. Commercial CMP simulation software is available from companies such as Praesagus [9]. In our current implementation, we use a CMP simulation model derived from the Ph.D. thesis of Tugbawa [10]. The results we describe here have been previously reported at PMJ-2005 [2].

To validate the electrical impact of the TOPC methodology, i.e., in achieving more accurate performance analysis, we use a testbed consisting of three parallel 5000um semi-global lines in 90nm technology. After

CMP planarization we assume that there are three different heights (thickness values). Figure 2 shows metal lines with thickness values A, B, and C located at plus defocus, nominal defocus, and minus defocus, respectively. In this experiment, assuming a +/- 100nm thickness variation we have run simulations for nominal height (=0.35μm) as well as heights due to plus and minus defocus topography, 0.25μm, and 0.45μm, respectively. Table I has captured different possible scenarios and their corresponding results.

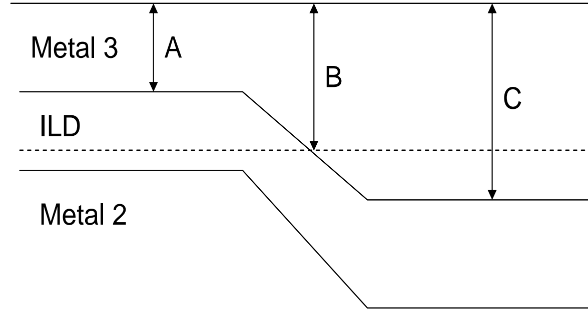

Fig. 2. Thickness variation after metal deposition.

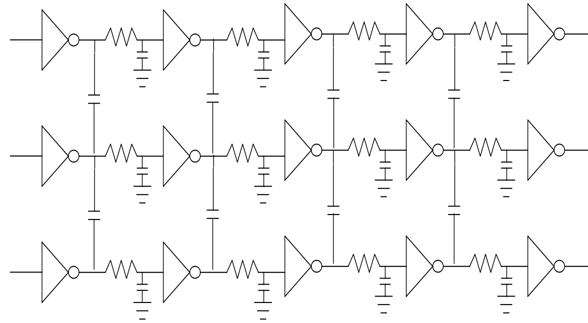

Fig. 3. Schematic of a buffered interconnect system

Figure 3 shows a system of three parallel buffered interconnect that is used in our experiment. Using the above parameters we configure our buffered interconnect system in *Synopsys HSPICE U-2003.09* to compute circuit delay. CD difference between SOPC and TOPC is +/- 4nm, +/- 7nm, +/- 22nm for +/- 30 *nm*, +/- 50*nm*,+/- 100*nm* thickness variation, respectively. Assuming a thickness variation of +/- 100μm, and three different heights we have considered 9 possible cases. According to the results in Table I, SOPC can result in timing error up to 12.4%.

TOPC			SOPC							
width	height	delay	width	height	delay	%diff	width	height	delay	%diff
140	250	2.429	162	250	2.752	-11.8	118	250	2.206	9.2
140	350	2.415	162	350	2.749	-12.1	118	350	2.180	9.7
140	450	2.427	162	450	2.770	-12.4	118	450	2.187	9.9

TABLE I

COMPARISON OF THE TIMING DELAY USING SOPC AND TOPC; THE UNITS FOR WIDTH, HEIGHT AND DELAY ARE *nm*, *nm*, AND *ps*, RESPECTIVELY

We apply our method to typical designs of metal layers to verify enhancement of DOF margin and CD control. Figure 4 shows the simulation results of a metal shape with 140nm line width and 90nm space. The

five curves from 0 to 0.4 represent OPC patterns applied to five different DOF models. CDs induced by the five different OPC patterns are plotted with the results of lithography simulation using 0.0μm to 0.6μm DOF models. With the SOPC (Standard OPC) method, if the pattern is located at 0.3μm topography and corrected with the 0.0μm OPC model, the pattern will violate CD tolerance, which is typically +/-10% of CD. In other words, if a pattern has topographic variation outside of +/- 0.3μm, or total DOF error (including wafer stage error) exceeds 0.3μm, then the pattern fails tolerance criteria and will contribute to yield degradation. On the other hand, if we apply TOPC with 0.3μm DOF model to the pattern, then we obtain an additional 0.1μm DOF within the CD tolerance.

Table II summarizes the experimental results. In this table, DOF range is the maximum DOF range of the pattern in a particular topography, which can be measured according to + and - directional DOF variation. For example, if a pattern is located at 0.2μm topography, + directional DOF ranges of the pattern are 0.05μm with SOPC and 0.12μm with TOPC. Thus, the pattern increases the + directional DOF range by 0.07μm after TOPC with 0.2μm DOF model, and the total DOF range of TOPC increases by 0.14μm compared to that of SOPC.

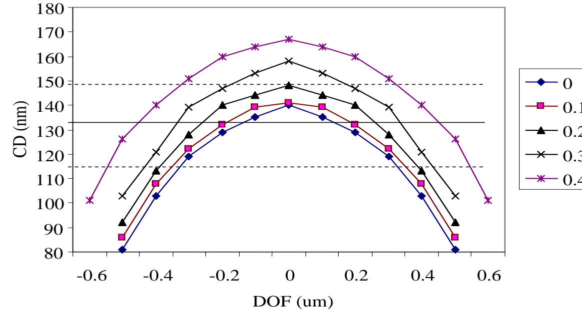

Fig. 4. Comparison of DOF and EPE improvements with 0.14μm line width and 0.9μm space.

OPC method	Topography (thickness: μm)	- directional DOF range	+ directional DOF range	Total DOF range
SOPC	0.0	0.25	0.25	0.50
SOPC	0.1	0.35	0.15	0.50
SOPC	0.2	0.45	0.05	0.50
SOPC	0.3	0.48	0.00	0.48
TOPC	0.0	0.25	0.25	0.50
TOPC	0.1	0.38	0.18	0.56
TOPC	0.2	0.52	0.12	0.64
TOPC	0.3	0.49	0.09	0.58

TABLE II
COMPARISON OF DOF MARGIN WITH TOPC AND SOPC.

With an experimental testbed of 90nm foundry libraries, industry OPC recipes, and commercial OPC and ORC (Optical Rule Check) software tools, we have confirmed that our technique achieves up to 67% reduction in edge placement errors at worst-case defocus. In particular, TOPC can achieve up to 74% worst-case printability problem reduction such as notching and bridging of patterns. Our research on the electrical impact of purpose method shows that the timing uncertainty is reduced. Also, lithographic process window is one of the most important reasons for stringent requirements for the CMP and dummy fill processes. A topography-aware OPC flow will enable reduction in layout density control requirements, and hence the design impact (e.g., capacitive coupling overhead) of dummy fills. In addition, the electrical impact of our proposed TOPC method is investigated. The results show that TOPC can significantly reduce timing uncertainty in addition to process variation.

B. Post-Lithography Sign-off for Wires

PLSw is a general technology that can account for deviations between drawn and printed shapes, not only in the $x-y$ plane, but also in the z dimension. With scaling geometries and manufacturing process not keeping up, discrepancy between shapes drawn by the designer and those printed on wafer is growing. As a result, modeling of and accounting for these process variations becomes an important component of current and future design flows. Thorough process wafer shape simulation, interconnect electrical parameters such as resistance and capacitance can be estimated more accurately.

A methodology for estimating interconnect performance from wafer shape contours of interconnect rather than drawn layout may become a necessary step in future performance sign-off flows. These wafer shapes can be obtained by lithography simulation. Such performance estimation is complicated by the fact that simulated contours need not be rectilinear and may be arbitrarily complex. Moreover, such estimation may be done at multiple process (focus, exposure, etc.) points to assess the robustness of the interconnect performance to process variations.

We have investigated a full-chip interconnect analysis flow which takes simulated non-rectilinear interconnect shapes (e.g., from lithography simulation) as input, and computes interconnect parasitics to feed into standard delay calculation and timing analyses. Figures 5 and 6 show preliminary results for a chip layout in 90nm process technology. Figure 5 (respectively, Figure 6) shows the fraction of M2-layer wire segments whose extracted resistance (respectively, capacitance) change by a given amount when actual litho-simulated shapes are taken into account. Our results indicate as much as 20% change in interconnect resistance, and up to 10% change in interconnect capacitance.

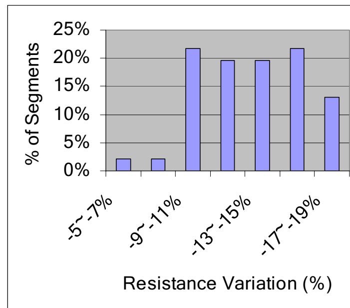

Fig. 5. Resistance variation.

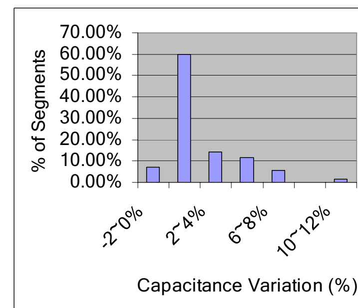

Fig. 6. Capacitance variation.

III. Manufacturing Non-Idealities and Interconnect Performance

Manufacturing non-idealities can occur in the *x-y* plane due to OPC error and process variation, in the z dimension due to nonuniform planarization, and along the sidewall of a wire due to etch. In this section, we discuss the impact of conductor sidewall non-idealities and a simple "equivalent-width" methodology to compensate for such non-idealities.

In typical etch processes (plasma, ion, RIE), different pattern density leads to different consumption of etchant, which in turn leads to sidewall angle variation [3]. Figure 7 illustrates the cross-section of a conductor before and after the etch process. Since OPC can not fix all proximity effects, actual fabricated patterns are different from the original design. To accurately account for these geometric changes, commercial extraction tools (e.g., *Synopsys Star-RCXT*) have special features that allow the sidewall angle to be modeled [4].

We motivate our discussion with Figure 9, which shows the impact of non-zero sidewall angle on total capacitance of a wire. The figure is obtained by studying a system of two conductors, C and C', with C to the left of C'. We vary the right sidewall angle of C, and the left sidewall angle of C'. We then capture

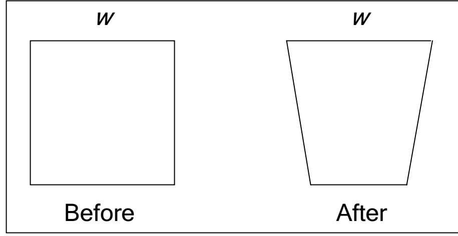

Fig. 7. Interconnect cross-section before and after etch.

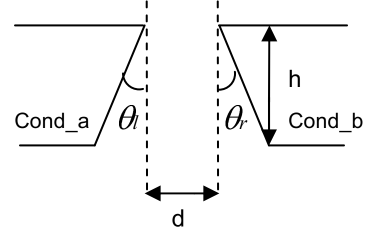

Fig. 8. Conductors *a* and *b* with non-vertical sidewalls (i.e., non-zero sidewall angles).

the changes in total capacitance of conductor C. The *Synopsys Raphael V-2004.06* three-dimensional field solver [8] is used to extract the capacitance components of these configurations. In Figure 9, C_{NT} and C_T respectively denote the total capacitance with non-vertical sidewalls, and the total capacitance with vertical sidewalls. According to the figure, the total capacitance of C can decrease by more than 10% when its sidewall angles are greater than or equal to seven degrees.

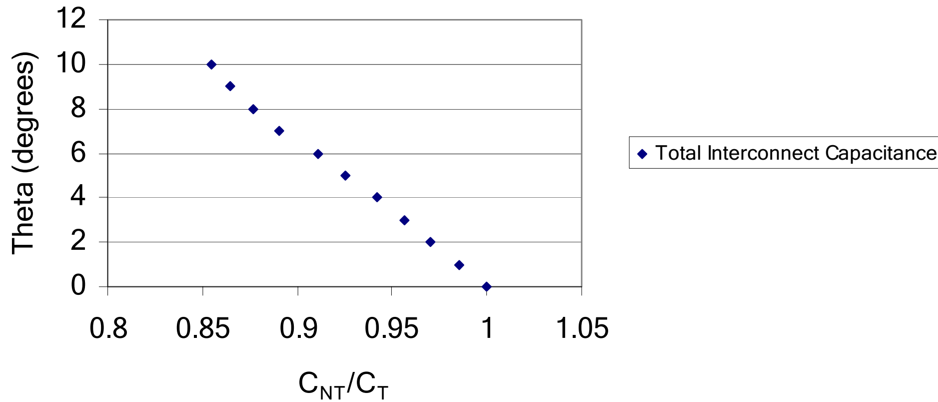

Fig. 9. Sidewall angle θ versus the ratio C_{NT}/C_T.

With successive technology nodes, and with the difficulty of reducing interconnect pitch, the semiconductor industry has seen a steady increase in maximum conductor aspect ratio [6]. As a result, fringing capacitance (capacitance between conductor sidewalls and substrate or neighboring-layer conductors) becomes an ever-more significant component of total capacitance. Figure 8 shows that non-vertical sidewalls imply a capacitance between *non-parallel* (sidewall) plates. In the figure, h is the height of the conductor and d is the distance between the two conductors with vertical sidewalls. We use θ_r and θ_l to respectively denote conductor a's and conductor b's sidewall angles.

A simple analysis shows that capacitance between the non-parallel plates (cf. Figure 8) can be calculated according to Equation (1):

$$C = \int_0^h dC = \int_0^h \frac{\varepsilon l dx}{d + x tan\theta_l + x tan\theta_r} = \frac{\varepsilon l (ln(d + h(tan\theta_l + tan\theta_r)) - ln(d))}{tan\theta_l + tan\theta_r} \quad (1)$$

According to Equation (1), the capacitance between two non-parallel plates is a logarithmic function of the inter-conductor distance. Furthermore, as the sidewall angle increases, the bottom width of the conductor decreases; along with the changes in conductor width due to wire aspect ratio, this will change the ground capacitance. Logarithmic functions can be approximated by a linear function over a small domain. Hence,

to appropriately account for the capacitance components of interest (i.e., total and coupling) we use the average of the top and bottom width of the wire as its new *equivalent-width*, as given in Equation (2):

$$w_{eq} = \frac{w_{top} + w_{bottom}}{2} \tag{2}$$

where w_{eq}, w_{top} and w_{bottom} respectively denote the equivalent-width, the top width, and the bottom width of the wire. Note that equivalent-width is linearly dependent on the top and bottom widths of the conductor, which implies a linear dependence on inter-conductor spacing for any given pitch.

To validate the simple equivalent-width methodology we have performed simulations using the system of conductors portrayed in Figure 10.

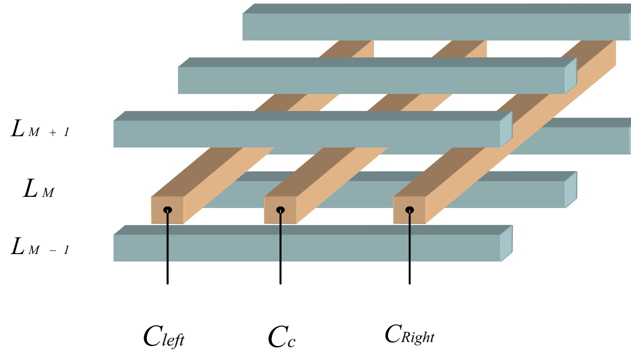

Fig. 10. Schematic view of the simulation configuration.

We vary the two sidewall angles of C_c, the right sidewall angle of C_{left}, and the left sidewall angle of C_{right} from 0 to 10 degrees in steps of one degree; there are a total of 14641 combinations of sidewall angles. We use *Synopsys Raphael V-2004.06* [8] to obtain Figure 11, which shows the distribution of the percentage error of the total and coupling capacitances across all the configurations. According to the figure, replacing each configuration having non-zero sidewall angle with the corresponding equivalent-width configuration will preserve total and coupling capacitances to within 2% and 2.5% of their nominal values (with non-vertical sidewalls), respectively.

IV. Impact of CMP Fill on Interconnect Performance

Chemical-mechanical planarization enables multilayer interconnect architectures. To enhance uniformity of post-CMP wafer topography, dummy fill is inserted to improve the uniformity of (effective) feature density. However, while dummy fill insertion improves feature density uniformity, it also changes coupling and total capacitance of functional interconnects [7], [11], [12].

In this section, we first study the impact of floating and grounded metal fill shapes on coupling (C_c) and total (C_{tot}) interconnect capacitance, in the context of various metal and fill configurations. We then motivate and outline an "intelligent fill synthesis" methodology that may be appropriate in future technology nodes.

A. Modeling of Fill Patterns

In the following discussion, the following notation is used.

- w_m: Line width
- h_m: Metal height
- h_{ild}: Dielectric height
- l_f: Fill length
- w_f: Fill width
- h_f: Fill height

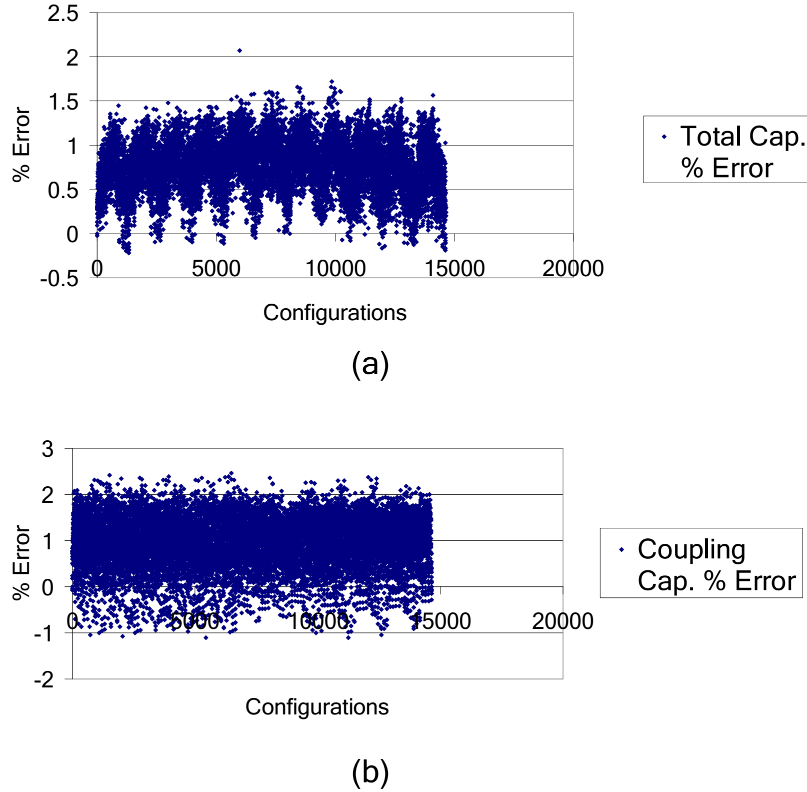

Fig. 11. (a) Total capacitance % error distribution. (b) Coupling capacitance % error distribution.

- s_x: Horizontal spacing between fill features
- s_y: Vertical spacing between fill features
- d_{ko}: Keep-out distance

Our experiments with floating fill shapes assume rectangular, isothetic fill features aligned horizontally and vertically as shown in Figure 12. In the figure, conductors *A* and *B* are active interconnects, and the metal shapes between them are dummy fills. We consider the cases of one, two and three columns of fill features between the active interconnects.

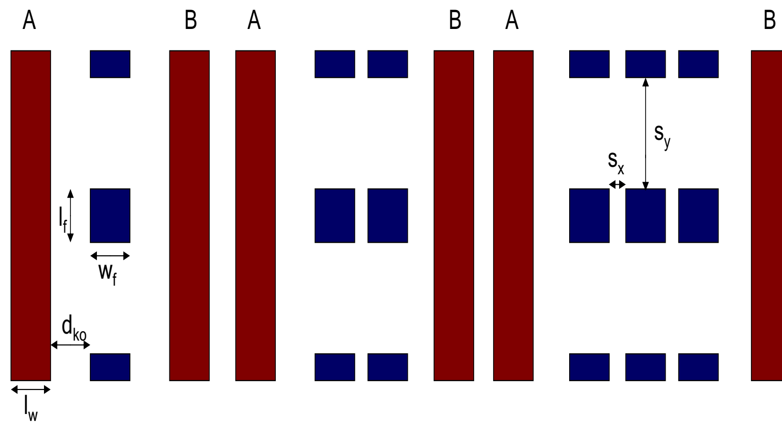

Fig. 12. Floating fill pattern examples.

We study the impact of the fill/wire parameters l_f, w_f, h_f, s_x, s_y and h_m on coupling capacitance C_c between the active interconnects, and on total capacitance C_{tot} of a single active interconnect. In our simulation configuration the interconnect layer is sandwiched between two ground planes. Specifically, we determine changes of C_c and C_{tot} with respect to each of the parameters of interest, across the three configuration cases (i.e., with one, two and three fill columns). As expected, increasing the number of columns slightly increases the total capacitance (up to 0.17%) and significantly reduces coupling capacitance (by up to 99%). In our experiments we use nominal values of $0.4\mu m$ and $0.2\mu m$ for metal thickness and metal width, respectively.

Figure 13 shows changes of C_c/l versus fill length, where l is the interconnect length, and also captures coupling capacitance changes as we increase the number of fill columns. Figure 14 plots changes of C_{tot}/l with respect to fill length. Such simulation studies can confirm simple guidelines for selection of a "good" fill pattern (cf. [7]), e.g.:

- If the number of fill rows is fixed, then we should use as many fill columns as possible.
- If the number of fill columns is fixed, then we should use as few fill rows as possible.

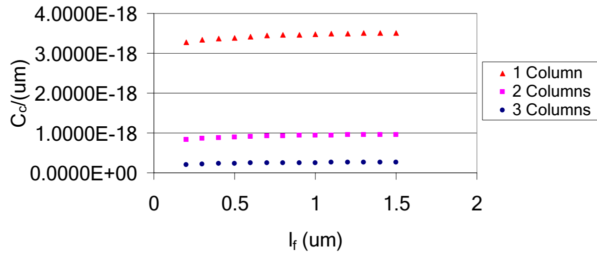

Fig. 13. Variation of coupling capacitance between active interconnects with respect to fill length.

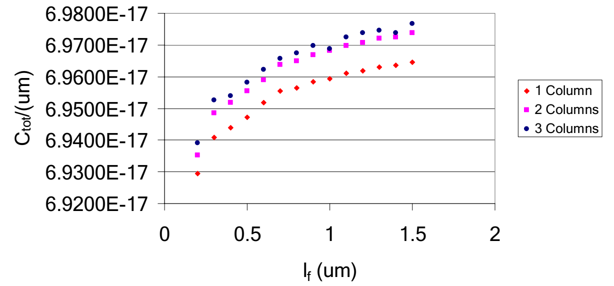

Fig. 14. Variation of total capacitance of an individual interconnect with respect to fill length.

Figure 15 plots C_c/l with respect to fill width, while changes in C_{tot}/l with respect to fill width are shown in Figure 16. We see that fill width has substantial impact on C_c (up to 38%), but insignificant impact on C_{tot} (no more than 0.50%).

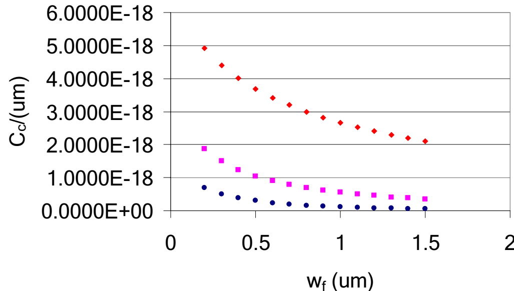

Fig. 15. Variation of coupling capacitance between active interconnects with respect to fill width.

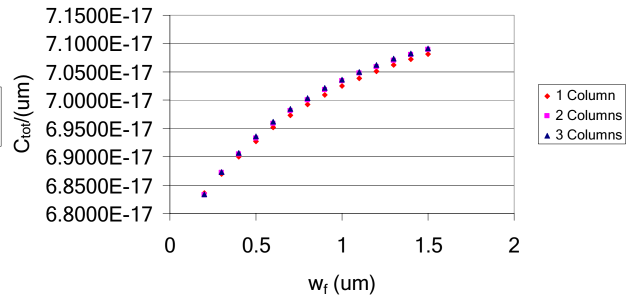

Fig. 16. Variation of total capacitance of an individual interconnect with respect to fill width.

Other experiments with grounded fill shapes are relevant to the regime where dummy vias are used along with dummy metal-layer shapes to create "tied and stacked" fill. Tying to ground or power traces eliminates floating metal that can attract potentially harmful stray charge and/or facilitate noise coupling between interconnects. Stacking of fill shapes using via fill improves mechanical stability of low-k dielectric layers, among other benefits. Our studies of grounded fill use the configuration shown in Figure 17. In the figure, conductor A is the active interconnect, and metal shapes on either side are dummy fill.

In our grounded fill experiments, we insert a grounded fill into the configuration of Figure 17, and capture the changes in total interconnect capacitance. We perform this experiment in the context of the same fill

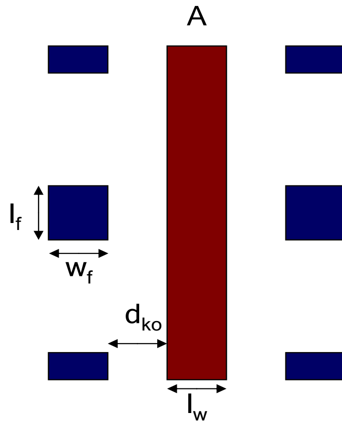

Fig. 17. Grounded fill pattern example.

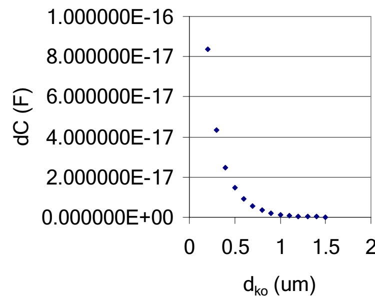

Fig. 18. Change in total interconnect capacitance due to insertion of a grounded fill shape, versus keep-out distance.

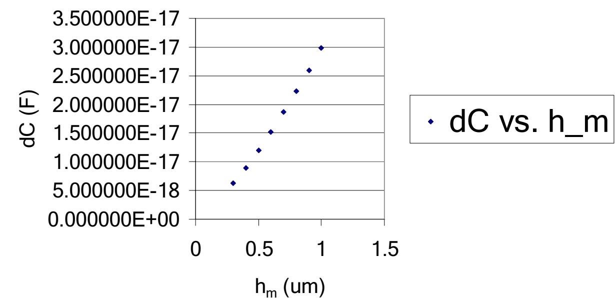

Fig. 19. Change in total interconnect capacitance due to insertion of a grounded fill shape, versus metal height.

and wire pattern configurations as in our floating fill experiments. Figures 18 and 19 illustrate how fill/wire geometries can potentially change the total interconnect capacitance. Figure 18 shows the change in total capacitance of a wire due to insertion of a grounded fill shape; this change is plotted against keep-out distance. Figure 19 plots the same total capacitance changes with respect to metal height.

B. Intelligent Fill Synthesis

As the industry moves toward the 65nm node and beyond, traditional fill synthesis methods reach their limits of usefulness. One indication of this is the emergence of so-called "recommended rules", e.g., "it is better to have a small difference between the density values of adjacent windows", or "it is better to maximize the overlap of fill shapes on adjacent layers to enable dummy via insertion". Of course, the impact of fill synthesis on timing continues to be a key concern for the designer. It is increasingly difficult for a DRC platform to obtain an *optimal, design-driven* fill synthesis solution that meets all basic CMP design rules and as many recommended rules as possible, while minimizing the impact on timing. In this subsection, we sketch the anticipated features of a more sophisticated, dedicated CMP fill synthesis tool - *intelligent fill synthesis* - that can potentially reduce engineering effort while enhancing manufacturability (by increasing process and design latitudes). We believe that intelligent fill synthesis must embody such features as the following.

- *Multilayer Density Control:* Post-CMP deposition of oxide in the back end is conformal; therefore, the topography variation in one layer is almost directly transferred to the upper layer, and the topography variation of the upper layer is added to that from the previous layer. Even when the density variation

of one layer is small, it is possible to have large enough variation for the entire back-end stack to cause yield loss or to exceed depth-of-focus limits of lithography. Intelligent fill synthesis should perform concurrent minimization of the density variation of multiple layers, as well as that of each individual layer. Conventional fill synthesis methods cannot today perform such a task.

- *Model-Based Fill Synthesis:* Rule-based fill synthesis is based on concepts such as density or keep-out distance rules, which are applied to wiring segments that have less than certain threshold amounts of timing slack. Model-based fill synthesis, on the other hand, would use CMP models to, e.g., identify regions where planarity is important (next to heavily loaded critical segments and below critical segments). The model-based approach has implicit tight coupling to a timer, and models the impact of fill on coupling capacitance.
- *Timing-Driven Fill Synthesis:* One of the largest concerns in fill synthesis, apart from meeting the CMP design rules, is the impact of fill insertion to the capacitances of the existing nets. An excessive increase in wire capacitance can cause a net to violate its setup timing constraint. A large value for keep-out distance reduces this danger but it erodes into available areas to insert fills and sometimes makes it impossible to meet the minimum density constraint. With timing-driven intelligent fill, the impact of inserting fills on timing is continually assessed, and the minimum keep-out distance for each net to meet the setup time constraint can be computed to avoid a wastefully large "one size fits all" keep-off distance. In a more advanced, intelligent timing-driven fill flow, the impact of fill insertion on both wafer topography and timing would be analyzed and optimized concurrently. One additional advantage of timing-driven fill is that it can improve the hold-time slack of a net by deliberately and selectively introducing capacitance to that net.
- *Wire Sizing:* Changing the width of a wire has certain impact on the parasitics of the wire such as resistance and capacitance. For example, in an organic low-k/Cu system, widening a wire may result in reduced resistance not only because the wire gains width but also wider wire suppresses metal thickness loss. To complement the execution of timing-driven fill, it is possible to bias the wires by some small amount ($< 10\%$) and gain small timing slack. This will increase the operating latitude of the circuit. Alternatively, the impact of the height variation of wires can be compensated by width sizing to tighten the distribution of wire parasitics for any given drawn width.

In Figure 20 we sketch a practical approach to *intelligent* timing-driven fill.

Timing-Driven Fill
Loop:
0. Set an initial conservatism factor
1. Do (initial) RCX and STA
2. Identify timing-violating nets (TVNs) - i.e., timing-critical nets
3. Apply conservative net-protection (+keep-out distance and blocking $M+1/M-1$ layers) per TVN segment
4. Run (incremental) MC-Fill → target fill amount
5. PIL-FILL Synthesis:
5.1 Greedy insert fill in fill slack columns, targeting most-needy tiles and largest and largest-slack nets first
5.2 After K fill shapes have been inserted, re-run (incremental) STA based on ΔC's
5.3 Iterate until all required fill has been inserted (or, until no timing constraint looks safe)
6. Update Conservatism
6.1 Analyze windows that violate *min* constraints
6.2 Identify nets that belong to the windows that violate the constraints
6.3 Do (incremental) RCX and STA to change the conservatism factor of TVNs (return to Step 2)

Fig. 20. Timing-driven fill synthesis approach.

V. Conclusions

In this work, we have first studied the impact of two manufacturing process variation sources - wafer topography and sidewall angle - on the design process. For wafer topography variation, we present a practical methodology to reduce the impact of these variations. In the case of non-zero sidewall angles, we present an accurate modeling technique which considers the geometrical changes of the interconnect so as to accurately approximate its capacitance. This work has also studied the impact of floating and grounded dummy fills on coupling and total interconnect capacitance. Finally, we have described elements of "intelligent fill synthesis" and how such a capability could be deployed in a timing-driven CMP fill methodology. Our ongoing research studies the fundamental question of where in the design and manufacturing flows should intelligent fill synthesis be most effectively deployed.

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