The Road Ahead

Scaling: More than Moore's law

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IN TODAY'S FAST-CHANGING world, discerning "the road ahead" is more difficult than ever. For IC design and test, the road ahead has long involved various corollaries of the 50+-year scaling phenomenon known as Moore's law. Historically, Moore's law has been framed with respect to cost (microcents), density or functionality (bits per square millimeter), and performance (megahertz, megaflops). But for the foreseeable future, success of the semiconductor and electronics industries will require scaling of different elements: *value*, and *integration*. The dimensions of these latter components are not so obvious.

The Executive Summary of the *2009 International Technology Roadmap for Semiconductors* (http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_ExecSum.pdf; p. 18) provides a taxonomy of scaling in the traditional, "More Moore" sense.

- *"Geometrical (constant field) Scaling*—refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- "*Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)*—refers to 3-dimensional device structure ('Design Factor') improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- "*Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)*—refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity."

The ITRS Executive Summary elaborates further on *design equivalent scaling*, which is the burden that design technology must shoulder as process technology scaling becomes more expensive and less predictable: "Examples (not exhaustive) are: design-for-variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multi-core SOC architectures.... [It addresses] the need for quantifiable, specific design technologies that address the power and performance tradeoffs associated with meeting 'More Moore' functionality needs; and may also drive 'More Moore' architectural functionality as part of the solution to power and performance needs."

Never before in the history of the ITRS has the importance of design technology innovation to continuation ("more") of Moore's law been so clearly highlighted. But even as More Moore becomes increasingly challenging, it has become obvious that mere straight lines on log plots do not equate to market success: as this column has pointed out in the past, human psychophysical limits, Claasen's law of logarithmic utility, and other factors conspire to set the innovation bar considerably higher. Enter the concept of More than Moore.

Functional diversification is defined in the 2009 ITRS as "the incorporation into devices of functionalities that do not necessarily scale according to 'Moore's Law,' but [provide] additional value to the end customer in different ways. The 'More-than-Moore' approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution."

With regard to the role of design technologies, the ITRS further states, "Design technologies enable new

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functionality that takes advantage of More than Moore technologies. Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology." Truly, a new era has dawned when "software" is called out as an underlying technology for scaling the semiconductor roadmap!

What are the implications of "More than Moore" for the road ahead? My friend and ITRS Design technology working group co-chair, Juan-Antonio Carballo of IBM, helped me articulate the following thoughts, which bring us back to those new keywords, *value* and *integration*.

Above all, necessary design, CAD, and packaging advances needed to continue scaling will be focused on integration. Only part of this integration has to do with process; much of it has to do with design. From the product standpoint, scaling will increasingly be with respect to value derived from (a) functions and (b) their performance (e.g., cell phone data service at 4G speeds). Scaling that value requires both Moore (lithography-driven) and non-Moore ("passives"-driven, or functional diversification) types of scaling. In such a future, the traditional (litho-driven) scaling dimension becomes an ever-smaller portion of product scaling, as more of the product value is derived from a different dimension—interaction with the world (antenna, screen, energy sensing/capture, information input)—and as more system performance is derived from levels above the component level (system, software, etc.) and from the components that implement the product's interaction with the world.

At the same time, manufacturing process will remain a key to both scaling dimensions, but in very different ways: litho or "horizontal" device scaling on the one hand, and passives or "vertical" scaling on the other. In the era of integration, CAD and packaging innovation will become increasingly crucial differentiators, and will need to support both scaling dimensions proportionally. Accordingly, several key innovations over the next decade will concern massive integration of multitechnology elements that include software, sensors, actuators, and elements of conventional digital computing, communications, and storage. Such innovations include, on the CAD side, software design automation, packaging design automation, and multiphysics simulation capabilities. On the packaging side, necessary innovations include 3D integration, multitechnology packaging, and massive memory and software integration.

In closing, the road ahead has become a many-lane superhighway—one on which semiconductor and electronics companies will pass up their competition only to the extent that they successfully scale integration and value. Technologists will continue to push the frontiers of circuits (subthreshold and near-threshold design, multiradio smarts and interfaces), systems (spatially adaptive ultra-low duty-cycled), and processing (driven by parallelizable applications). At a higher level, any list of fundamental keywords will undoubtedly include *memory*, *interconnect*, and *3D*. And while traditional photolithography-driven scaling to below 20nm is unclear, equivalent scaling will come from software, stacking, architecture, and the other More than Moore technologies. There will be many fascinating "megatrend" trajectories to keep track of:

- *applications* (still driven by mobility, bio, cleantech, leisure—including portable multimedia, graphics resolution, core network bandwidth, photovoltaics, and . . . well, how would *you* bring together location sensing, network connectivity, motion sensing, image analytics, and security?),
- *massive storage* (e.g., a terabyte of Flash memory in a cell phone),
- *human-machine interaction* (intelligent, cognitive and natural, augmenting reality with virtual worlds), and
- *power and energy* (harvesting, management, portability).

Certainly, fodder for many more musings on The Road Ahead. ■

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