The Road Ahead

How much variability can designers tolerate?

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TRADITIONALLY, designers hate large variations in a gate's critical dimensions (CDs) because large variations imply large guardbanding in design (a ±25% guardbanding for timing is not uncommon). Lithographers hate small variations in CD numbers because they imply impossible process windows. With this December's publication of the *2003 International Technology Roadmap for Semiconductors* (ITRS), gate CD control requirements for lithography and front-end (etching) processes will doubtless receive intense scrutiny.

The specification "10% 3σ CD control (post-etch)" has long been a technology requirement, dating back to the mid-1990s *National Technology Roadmap for Semiconductors*. In recent editions of the *ITRS*, this requirement has "no known solution" even in the near term. Why, then, has this requirement remained so immutable?

Less variability is nice …

For integrated device manufacturers with high-value, high-volume products on leading-edge processes, even slightly better bin splits can mean significantly more dollars per wafer. Microprocessor companies in particular tend to see two trends:

- High-frequency designs have fewer gate stages in signal paths, and less averaging of variation means a greater impact of variation on timing.
- Exponential dependence of leakage power on process parameters (gate length, oxide thickness, and threshold voltage) means that high-end parts (containing low-threshold, leaky devices for high performance) can exhibit 20× spreads of leakage power, versus performance spreads of approximately 35%.

Reducing gate CD variation can leave some breathing room for newer problems such as random dopant fluctuations. Better parametric yield is also useful to foundries, because it means better value delivered to their customers. But such added value becomes less significant with lower-volume, less-aggressive semiconductor products—or with the traditional ASIC business model.

All else being equal, achieving less variability is better. It would also be better if we could achieve world peace, an end to hunger, and low-cost space travel. Unfortunately, reality intrudes: Today, automatic layout, place and route, and manufacturing signoff are close to broken because of a flood of new ground rules not easily handled by detailed routers. Other realities include growing design risk, a proliferation of pages in manuals devoted to design rules, and an exponential growth in several costs—for lithography R&D, masks, mask writers, and lithography equipment—that exceeds the Moore's law rate. Striving for unattainable levels of CD control does not come for free.

… But not essential

Preoccupation with gate CD control might be misguided for future technology nodes. In a recent communication, Edward Nowak observes that gate CD variation is rapidly becoming secondary to intra-die threshold voltage (V_t) variation as CMOS scales to 65 nm and beyond. This means that the 3σ variation in physical line width will not carry the same timing penalty formerly associated with such variation. Of course, there are limits: Gate lengths must be within some tolerance of nominal to keep the effects of capacitive-load mismatch and variation in short channels to below that of V_t variation. Budgets for intra-die gate-length variation

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could also rise significantly if designers can employ active V_t control (well biasing) to counter the mean value of short-channel effects on each chip.

There are also business reasons for avoiding unrealistic roadmaps for gate CD control. Above all, with today's rosy projections, there is little impetus for EDA companies to develop new techniques that design around large variations in gate CDs. Designers and design technologists should be more actively working in several areas:

- *Defining the effects of exposure and defocus variation.* These variations have a significant impact on isolated and dense layout features.
- *Developing a comprehensive understanding of leakage and how to control it.* This requires a better understanding of intra-die variation and its components, as well as new statistical power analyses. Improved leakage control will likely require a holistic use of multiple thresholds and supplies, and gate sizing and gate length biasing to complement logic and layout optimizations.
- *Understanding systematic variations.* Whether from lens aberrations, wafer bowing, the reflection of light from a lower-layer pattern, or the spinning on of a drop of photoresist, it is possible to model many process variations systematically. Comprehensive understanding, modeling, and simulation of such variations would permit designers to compensate for them in design.
- *Developing prevalidated, library-based design methodologies.* With better understanding of and compensation for variation, productivity scaling will permit new "library"-based solutions, from composable-in-context standard cells and IP blocks to strict constraints on layout (for example, permitting only one orientation and one pitch for poly gates).

Lithographers must more actively help the design, process, and mask communities; all of these communities must increase awareness of each other's requirements. Much of the following partial list has appeared in previous columns and recent publications:

- Reticle enhancement cost will be reduced if mask corrections are applied on a per-device basis, according to individual device performance windows. In general, designers must more fully communicate their intent and knowledge (of timing and yield goals, slacks, and sensitivities).
- Process windows must be statistical, rather than simple (rectangular) regions in exposure-defocus plots.
- Similarly, manufacturing must communicate any anisotropies in the process. Designers today do not care about distinctions between the orientations of die on a reticle, or even between horizontal and vertical orientations of layout features. However, equipment (such as scanners) might afford better control in a single direction.

Designers and design technologists must understand the interaction between solutions for different process layers.

Give me a number

Perhaps the next major revision of the *ITRS* in 2005 will finally contain a change in the 10% gate CD variation requirement. But if this happens, who should come up with the new number, and how?

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