The Road Ahead

The cost of design

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Most of us share general notions of *cost*. For example, cost offsets revenue to determine profits or losses. Cost can be a barrier to initiating research or development efforts. And lower costs are better than higher costs. Here, I examine the cost of design and its potential impact on the semiconductor industry roadmap.

Design as an NRE cost

For any semiconductor product, design is part of the nonrecurring engineering (NRE) cost—the fixed cost of development and production. As the semiconductor industry approaches the 100-nm technology node, manufacturing NRE (mask set and probe card) costs are nearing $1 million for a large IC. With an average of just 500 wafers produced from each mask set, rapid growth of manufacturing NRE can throttle the initiation of new IC design projects. However, design NRE costs, which routinely reach tens of millions of dollars, dwarf manufacturing NRE costs. Indeed, according to the 2001 *International Technology Roadmap for Semiconductors* (http://public.itrs.net), "Cost of design is the greatest challenge to continuation of the semiconductor roadmap."

Consider two factors that contribute to design cost. First, according to a model developed by Dataquest for the 2001 *ITRS*, the design cost per unit time per designer consists of $326,070 ($181,568 in 1990, increasing by 5% per year for the past 12 years) for the designer's annual salary and overhead, plus $157,159 ($99,301 in 1990, increasing by 3.9% per year) for annual tool costs per designer. This estimate ignores the costs of CAD integration and support, which are often several times the tool costs.

Second, the number of designer months (number of designers times total time) in a design project is increasing rapidly. The well-known design productivity gap between growth in designer productivity (number of transistors per designer month) and growth in number of available transistors on a given-size chip—originally estimated by Sematech in 1994 to be increasing at 37% per year—is still growing today. Assuming a team of 20 designers can reliably complete a multimillion-gate design in one year, the design NRE cost is still nearly $10 million.

Cost of uncertainty and risk

During the product creation process, manufacturing turnaround times are on the order of weeks or months with relatively low uncertainty, whereas design turnaround times are on the order of months or years with high uncertainty. (Design errors also lead to silicon respins that multiply manufacturing NRE costs.) Uncertainty in design turnaround time translates directly into uncertainty in time to market.

Aurangzeb Khan, executive vice president of Simplex's SoC Design Foundry, assigned a dollar value to this problem. In his presentation at the 2002 Design Automation Conference, Khan said a three-month delay in the time to market of a high-value, high-volume application could cost $500 million. So, when product life cycles are well below one year in several key consumer markets, designers must consider uncertainty and risk as part of the design cost.

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11th Asian Test Symposium (ATS 02)

18-20 November 2002
Guam
http://ats02.ip.elec.mie-u.ac.jp

The Asian Test Symposium provides a forum for engineers and researchers worldwide, and especially from Asia, to present and discuss various aspects of system, board, and device testing with design, manufacturing, and field considerations in mind. TTEP is offering tutorials in conjunction with the symposium.

3rd Workshop on RTL and High-Level Testing (WRTLT 02)

21-22 November 2002
Guam
http://www.ip.elec.mie-u.ac.jp/~wrtlt02/

WRTLT brings together researchers and practitioners of large-scale integration testing to exchange ideas and experiences on register-transfer-level (RTL) and high-level testing. Held in conjunction with ATS 02, this workshop will provide a discussion forum for the coming age of SoC devices. Topics include functional-fault modeling, RTL automatic test-pattern generation, RTL DFT, RTL BIST, the relationship between RTL and gate-level testing, high-level approaches for testing, and SoC testing. The deadline for submissions is 31 July 2002.

16th International Conference on VLSI Design (VLSI 03)

4-8 January 2003
New Delhi, India
http://vlsi.ccrl.nj.nec.com/~chak/vlsi2003/index.html

Conference topics include all aspects of IC design, technology, and related CAD.

6th International Workshop on the Economics of Design, Test, and Manufacturing

8-10 January 2003
Hong Kong

This workshop provides a forum for discussing and exploring current and future design, test, and manufacturing trends. With the theme, "driving the cost down," the workshop will address how the cost of delivering increasingly complex microelectronic systems drives these trends. The primary focus will be on the economic impact of decisions directly associated with the design, manufacturing, test, and field maintenance of ICs, cores, SoCs, boards, and systems. The deadline for submissions is 15 September 2002.

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Cost of lost quality

Finally, there is the issue of design quality and value. A speed difference of 200 MHz separates salable microprocessors from scrap. Yield loss and die cost increase rapidly with area. Power affects package costs by about a dollar per watt. The 2001 *ITRS* observes that the design productivity gap may result in less new logic (differentiating value) per chip. And in *Closing the Gap Between ASIC & Custom* (Kluwer Academic, Norwell, Mass., 2002), David Chinnery and Kurt Keutzer note huge quality gaps (along the speed, area, and power axes) between what ASIC design teams achieve and what the silicon can actually deliver. Thus, another of design's costs is the value that it *fails* to extract from the process.

DESIGN PRODUCTIVITY—the value created by the design, divided by the cost of design—measures how well the semiconductor industry extracts value from manufacturing capability. When designers cannot predictably "fill the fab" with high-value, high-margin parts, there is less return on a foundry's capital investments, leading to workarounds (reprogrammability, platform-based design, software-based product differentiation, and so on) that provide value through means other than silicon differentiation. Such workarounds sacrifice quality and value in designs, meaning fewer design projects are worth attempting. Thus, design and process technologists are in the same boat, trying to maintain the retooling cycles that are the heartbeat of the semiconductor roadmap. Cost of design is indeed the semiconductor industry's greatest challenge. ■

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