

Conference Reports

8th International Mixed-Signal Testing Workshop

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IMS

Held annually in either Europe or North America, IMSTW offers engineers and researchers a major opportunity to discuss issues in mixed-signal testing and related areas. This year's workshop, held 18-21 June, will include an invited keynote, regular papers, posters, a panel, and three short tutorials.

IMSTW addresses all aspects of testing and reliable design of integrated mixed-signal and mixed-technology circuits and systems. This includes testing and design verification of system-on-a-chip circuits, printed wiring boards, and systems on packages. The technology spectrum includes analog and mixed-signal design, microelectromechanical systems (MEMS), optics, and RF design.

The workshop venue this year is Montreux, the pearl of the Swiss Riviera. Montreux is on the Geneva Lake and crowned by the majestic Alps.

For more information, see <http://imstw.epfl.ch/>.

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The Road Ahead

continued from p. 120

circuit and layout topology, to let designs coexist with increased manufacturing variability. But broader, open questions include whether design goals should shift to value per wafer, in contrast to today's performance-centric objectives.

WHAT WILL HAPPEN to circuit performance and parametric yield when the gate length's 3σ variation is 10%? How about 15%, or even 50%? Will designers ever need to worry about such large variability? Consider the gate length component of variability in the *ITRS*. In a given *ITRS* technology node, the DRAM half-pitch is the typically quoted minimum feature size—130 nm in 2001. The *ITRS* also defines two additional numbers for a given technology node: printed gate length in resist (90 nm in 2001) and post-etching minimum physical gate length at the silicon interface (65 nm in 2001). Physical gate length is already just half of what is traditionally viewed as drawn channel length. Effective gate length, L_{eff} , is even shorter, due to lateral underdiffusion of source-drain extensions. In 2001 (the 130-nm technology node), if source-drain extensions accounted for 16 nm on each side (a value published by Intel), then L_{eff} was only $65 - 32 = 33$ nm.

The *ITRS* has set 10% of *physical* gate length as the technology requirement for the 3σ variability budget. Whether this degree of control is achievable is another story, but 10% of 65 nm in today's 130-nm technology node means 6.5 nm, or nearly 20% of L_{eff} , after accounting for source-drain extensions. If the source-drain extension distance does not scale with physical gate length, L_{eff} will decrease rapidly, magnifying physical gate length variability relative to L_{eff} . All in all, it's clear that design will have to mitigate extremely large device variability within the next few process generations. ■

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The Road Ahead

Variability

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■ **IC MANUFACTURING VARIABILITY** is critical to the design-manufacturing interface, which, along with productivity, power, interference, and error tolerance, ranks as a key cross-cutting challenge in the design technology roadmap.

Variability refers to deviations from nominal specifications, occurring across individual die, wafers, or lots. The inherent variability length scale ranges from subwavelength (interference in optical lithography) to microns (pattern-dependent loading effects in etching), to millimeters (lens aberrations and chemical-mechanical planarization). The *ITRS* (<http://public.itrs.net>) generally specifies the 3σ variation across all locations, in all chips, and in all lots. The *ITRS* states variability-control requirements for several parameters, including device (effective gate length and source-drain resistance), interconnect (via resistance, and global line width and thickness), and other manufacturing parameters (overlay, and so on).

Intrinsic variation occurs during IC fabrication and can be *systematic* or *random*. Systematic variation implies that known and predictable phenomena cause changes in parameter values such as effective channel length L_{eff} . Random variations are due to inherent unpredictability—for example, fluctuations in channel doping, gate oxide thickness, and interlevel dielectric permittivity. Because designers cannot compensate for random phenomena, this type of variability significantly threatens the design of nanometer scale circuits with adequate yields.

Dynamic variation arises during circuit operation and applies to parameters such as temperature and supply voltage. Although designers can model such variations during the design

process, these variations' transient nature makes compensating for them difficult. Thus, designers typically address dynamic variations through preventive measures, such as power network sizing that limits *IR* drop to 5% of V_{DD} .

Design technology mitigates systematic variability using aperture, phase, and pattern knobs. For example, optical proximity corrections (aperture knobs) and phase-shifting masks (phase knobs) can control diffraction and reflection effects in deep-subwavelength optical lithography. “Dummy” area fill (pattern knobs) can control copper dishing and erosion in planarization, and loading effects in etching. Such reticle enhancement techniques place a growing burden on physical design with respect to layout complexity and manufacturing (mask) nonrecurring engineering costs. For example, new, context-sensitive design rules challenge layout productivity. In addition, library generation, placement and routing, and physical verification flows must adapt to accurately model the effect of future area fill insertion on *RLC* parasitics. Static performance analysis tools must account for the fact that delay or noise values are no longer numbers, but distributions.

Design technology for variability will need to use additional knobs such as circuit topology. In logical and physical design, designers may need to acknowledge that not all devices are created equal. For example, devices at the reticle edge will have higher variability (or be of lower quality), even after reticle enhancement, than nominally identical devices at the reticle center. Some researchers have proposed incorporating *regularity* (the repeated use of relatively few known-manufacturable pattern elements) in both