Roadmaps and Visions for Design and Test

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AS YOU BEGIN READING this issue, the 2001 *International Technology Roadmap for Semiconductors* (http://public.itrs.net/) is being released. A core message of the *ITRS* is that the cost of design and test is the greatest threat to the continuation of the semiconductor roadmap. Cost ultimately determines whether value differentiation depends most on software or hardware, on a programmable commodity platform or a new IC. Design nonrecurring engineering (NRE) costs routinely reach tens of millions of dollars, and design cycle times take months or years. These far exceed manufacturing NRE costs and cycle times. Yet, investment in process technology has historically dominated investment in design and test technologies.

Since 1999, the *ITRS* has noted that design and test technologies face both silicon and system complexity challenges. Silicon complexity concerns process scaling effects and the introduction of new materials, or of device or interconnect architectures. Leakage, interference, process variability, and single-event upset reliability—as well as contexts such as silicon on insulator, mixed-signal system on a chip (SoC), and high-speed off-chip signaling—all significantly affect design and test needs.

System complexity arises from exponentially increasing transistor counts, which are enabled by smaller feature sizes and spurred by consumer demand for increased functionality, lower cost, and shorter time to market. Compounded with a diversity of IP sources, mixed technologies, and reuse contexts, system complexity causes many cost and productivity crises in verification and test, reuse, embedded software, and design processes.

The 2001 *ITRS* warns that design technology must increasingly share *red bricks* (technology requirements for which no known solutions exist) with other semiconductor supplier industries. An obvious example is the design-test interface, where built-in self-test and built-out self-test (BOST) must eventually enable test of analog and mixed-signal designs, test reuse, test of high-speed I/O, high-frequency designs, and so on. Other red bricks are shared with packaging, which needs design to deliver power management at all levels, from circuit to operating system and application software; and lithography and front-end processes, which need new design and test methodologies that maintain yield and value per wafer under increasing process variabilities. The challenge for design and test is to prove its value and return on investment to the rest of the semiconductor industry by providing solutions to such shared challenges.

This special issue opens with five personal perspectives from leaders in the design and test fields:

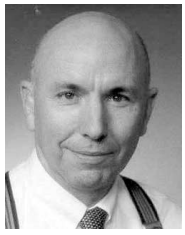
- Wojciech Maly describes the design and test cost problem and its solution: geometric regularity and reuse.
- Kurt Keutzer proposes programmability and programmable platforms as another workaround for crises in cost and turnaround time.
- Vinod Agarwal presents the promise of embedded test.
- Joseph Borel discusses the roadmap process and whether it is even identifying the right showstoppers.
- Raul Camposano describes the response of the EDA industry to technology drivers.

0740-7475/01/$10.00 © 2001 IEEE

The four articles, also from leaders in design and test, discuss various aspects related to the theme of this special issue. In the first article, "Power-Driven Challenges in Nanometer Design," Dennis Sylvester and Himanshu Kaul describe key challenges arising from silicon complexity, with a focus on leakage and power management. The second article, "Platform-Based Design and Software Design Methodology for Embedded Systems," by Alberto Sangiovanni-Vincentelli and Grant Martin, presents a vision for addressing system complexity through new methodologies for embedded software and platform-based design.

"A Mixed-Signal Design Roadmap," by Ralf Brederlow et al., describes the development of a mixed-signal roadmap newly introduced in the 2001 *ITRS*. This roadmap focuses on four key circuits and the required advances in their corresponding figures of merit. Finally, in "Strategies for Low-Cost Test," Rohit Kapur, R. Chandramouli, and T.W. Williams describe how the semiconductor industry can escape the trend of exponentially growing (relative to manufacturing cost per transistor) test cost per transistor.

WE HOPE this special issue inspires you in two ways. First, we hope you will look more closely at the 2001 *ITRS* and consider how the semiconductor industry roadmap process affects electronic design automation. Second, we hope this special issue will inspire renewed efforts to address the challenges and opportunities that face EDA today—both through partnerships with other semiconductor supplier industries and in the context of the overall trajectory of the semiconductor industry.



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