Futures and Core Algorithm Technologies for Physical Design

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Definitions

- Design
- Physical Design
- “Core Algorithm Technology”

Outline

- Contexts
- Drivers
- Disconnects
- Mindset changes / technology portfolio

Technology Context (NTRS)

- Semiconductor Industry Association National Technology Roadmap for Semiconductors
  - November 1994, renewal in December 1997
  - Roadmap for selves and competitors
- Defines the solution space
  - Devices → circuits → architectures → ...

SIA NTRS Technology Roadmap (1994)

Year		1995	1998	2001	2004	2007	2010
min feature		0.35	0.25	0.18	0.13	0.1	0.07
DRAM bits/chip		64.M	256M	1G	4G	16G	64G
¢x10 $^{-3}$ /bit		0.02	0.01	0.003	0.005	0.0005	0.0002
uP xtors/cm ^{2}		4M	7M	13M	25M	50M	90M
SRAM, bits/cm ^{2}		2M	6M	20M	50M	100M	300M
¢x10 $^{-3}$ /xtor		1	0.5	0.2	0.1	0.05	0.02
ASIC xtors/cm ^{2}		2M	4M	7M	12M	25M	40M
NRE ¢x10 $^{-3}$ /xtor		0.3	0.1	0.05	0.03	0.02	0.01
chip-to-pkg I/O		900	1350	2000	2600	3600	4800
clock	**on-chip**	300	450	600	800	1000	1100
(MHz)	**chip-to-board**	150	200	250	300	375	475

SIA NTRS Technology Roadmap (1994)

Year		1995	1998	2001	2004	2007	2010
min feature		0.35	0.25	0.18	0.13	0.1	0.07
chip size mm ^{2}	DRAM	190	280	420	640	960	1400
	uP	250	300	360	430	520	620
	ASIC	450	660	750	900	1100	1400
# wiring layers		4-5	5	5-6	6	6-7	7-8
supply V	desktop	3.3	2.5	1.8	1.5	1.2	0.9
	battery	2.5	1.8-2.5	0.9-1.8	0.9	0.9	0.9
max power	w/sink	80	100	120	140	160	180
(W)		5	7	10	10	10	10
	battery	2.5	2.5	3	3.5	4	4.5
min contacted	pitch	1	0.75	0.55	0.4	0.27	0.2
M1	H/W aspect	1.5:1	2:1	2.5:1	3:1	3.5:1	4:01
contact/via	logic	2.5:1	3:1	3.5:1	4.2:1	5.2:1	6.2:1
aspect	DRAM	4.5:1	5.5:1	6.3:1	7.5:1	9:01	10.5:1

(Overlay)

Company	AMD	DEC	IBM	Intel	TI	TI
Process	CS-44	CMOS-7	CMOS-6X	P856	C10	C07
Product	K6+	A21264+	PP60x+	Deschutes	n/a	n/a
On-Line	2H97	1H98	2H97	3Q97	1Q97	1Q98

(Overlays)

- Hand-drawn overlays showing major changes in NTRS between Nov. 1994 and June 1996

Technology Outlook

- Well-understood, moving fast
- Very costly game
- No roadblocks until << 0.10 μm
- Interconnect tuning is a big deal

Technology Implications

- Timing
- Signal integrity
- Power $\propto$ DSM
- Reliability
- Yield

Devices and Interconnects

- Weaker gates

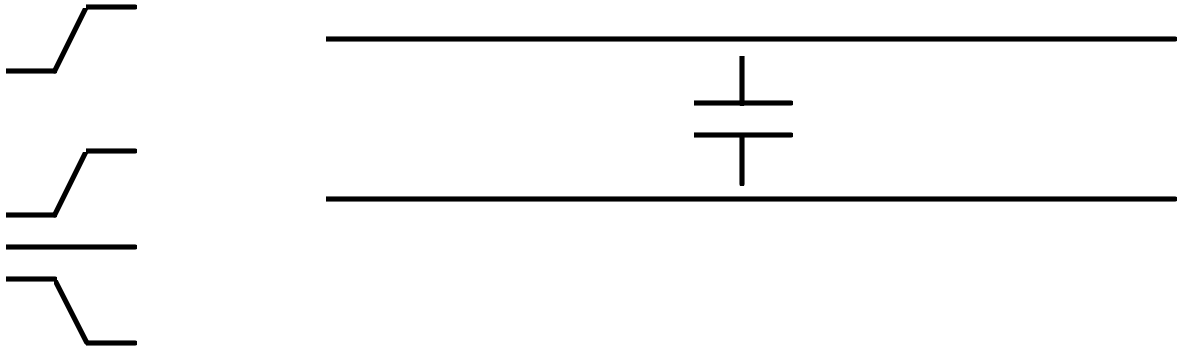
  delay (small_buf) = 120 ps + 1000 ps/pF
  delay (large_buf) = 600 ps + 200 ps/pF

- Higher RC in interconnect

nm	Ω/μm	fF/μm
350	0.15	0.17
250	0.19	0.19
180	0.29	0.21
130	0.82	0.24
100	1.34	0.27

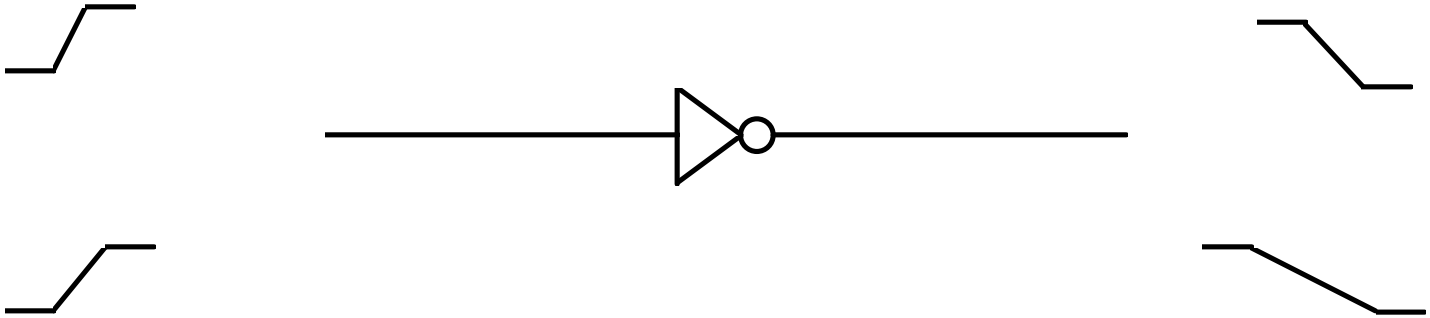
- Optimal scaling is unclear

Example



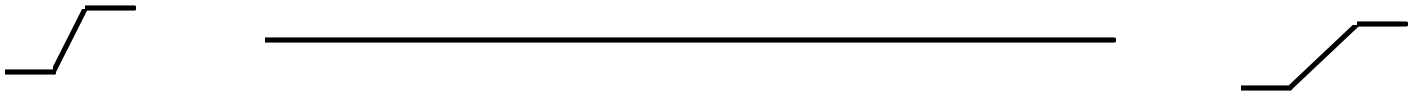
Coupling factor $\in$ [0 , 2]

Example



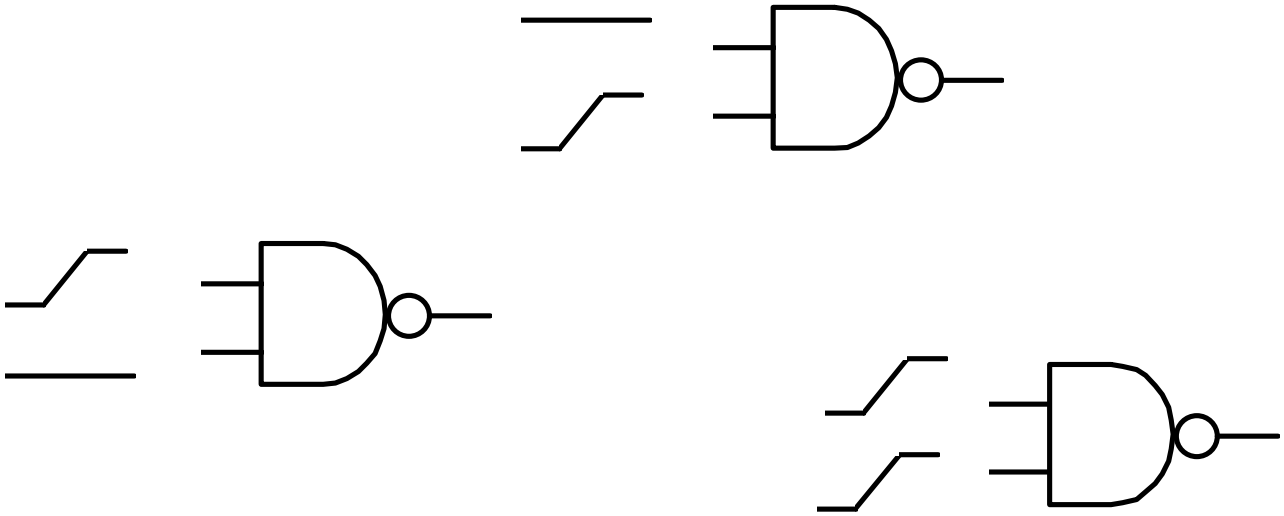
Input slew dependence

Example



Slew time degradation along a line

Example



Simultaneous switching and input ordering

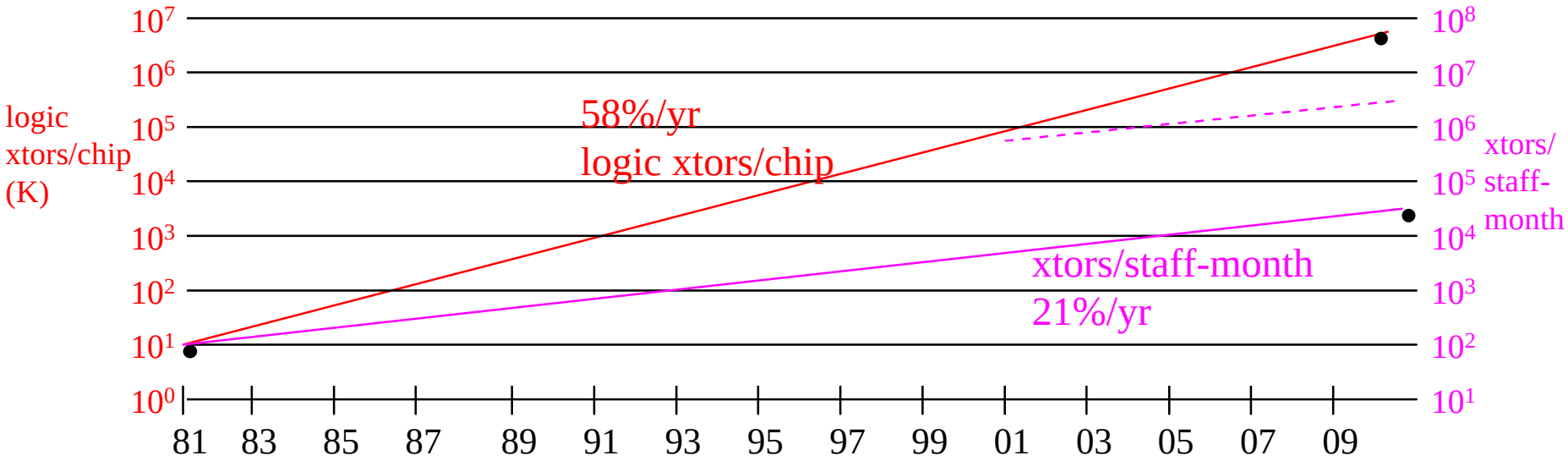
Technology Implications

- Design complexity
- Design complexity $\propto$ 1 / DSM
- Design complexity

Business Context

- Foundry starts ⇧
- Design starts ⇧
  - time-to-market = time-to-$
  - design productivity ⇩
- ⇨ Tool use and design methodology

Design Productivity Shortfall



Year	Technology	Chip Complexity	Staff Years	Staff	Staff Cost
1995	0.35um	5M	360	120	50M
1998	0.25um	20M	800	270	115M
2001	0.18um	80M	1800	600	260M

Foundry Starts 

- Not fab-limited
  - increased COT
  - new handoff models
- Foundry amortization
  - n-layer metal for complexity, density, $/wafer
  - yield becomes a driver

Design Starts ⬆

- Horizontal segmentation (design outsource)
- Reuse and HDL-based chip implementation

Tool use and methodology determinants:

- # turns matters
- good enough is good enough
- μarch/logic ⟷ logic/layout

Outline

- Contexts
- Drivers
- Disconnects
- Mindset changes / technology portfolio

Drivers

- Density / complexity
- I/O
- Reuse
- Frequency / mixed-signal
- Yield

Outline

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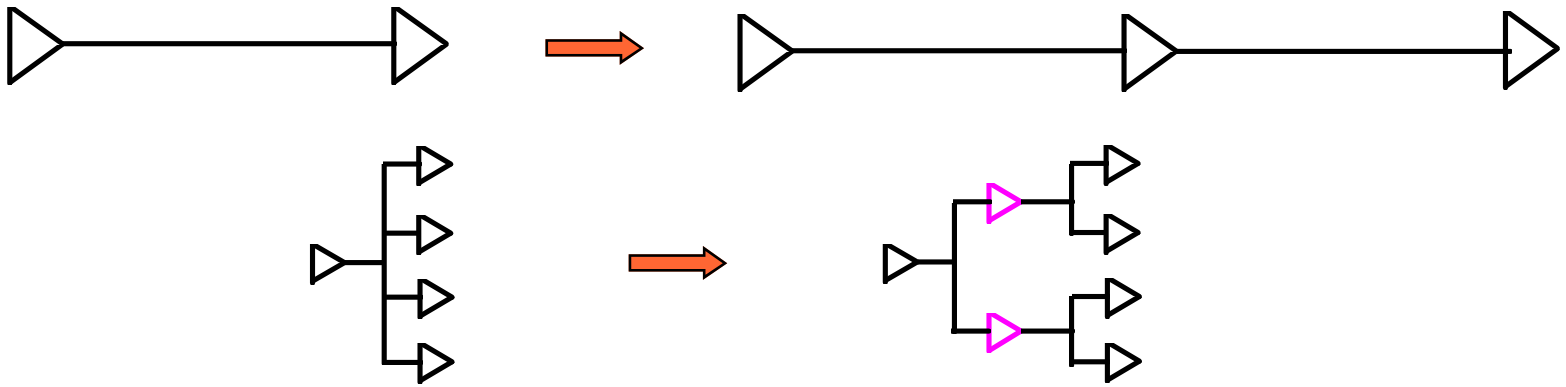
Disconnects

- Objectives
- Propagation of constraints, objectives
- Performance analysis
- Impedance mismatches
- Structure

Objectives

- Example: IPO/PBS
  - What are logic synthesis objectives ?
  - How does timing-driven layout respond ?
- Example: min-cut partitioning



Propagation of Constraints/Obj's

- Capture. Translate. Enforce.
- Example: "timing-driven placement"

  FP → time budgeting → WL-driven synthesis

  → (loop): slack budgeting → net delay UB

  → net cap UB → net length UB → net weight

  → clique model → placement

  (→ groute / droute / performance analysis / …)
- Close the loop !
-

Impedance Mismatches

- Example : accuracy in parasitic extraction
- Performance analysis context :
  - delay calculation : RSPF (no L), C_{eff}, input dependence, PVT derating, path-tracing, …
  - cell characterization
  - process variation
  - signal activity
  - (no detailed routing topology yet)

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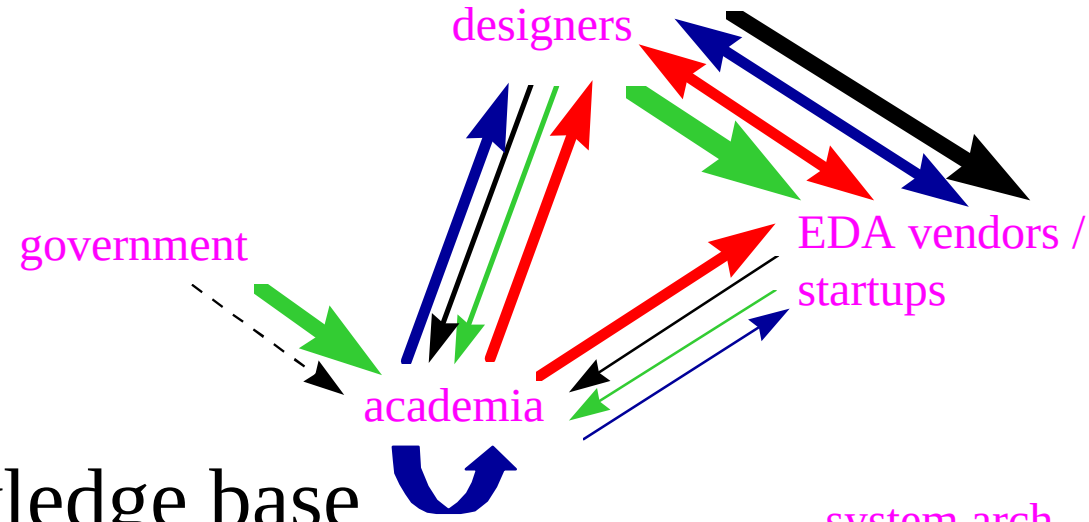
Structure

- Flows



people

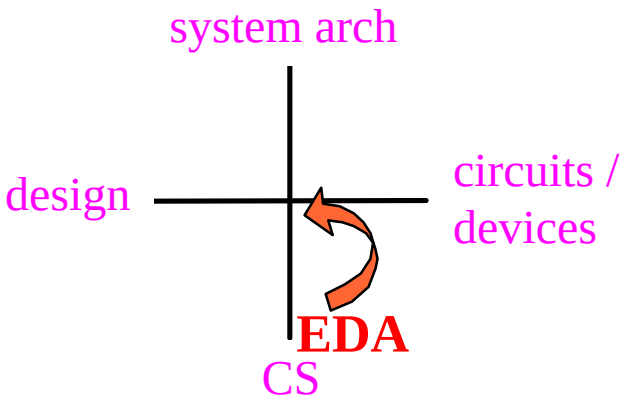
$$$

problems

technology

- Knowledge base

"Toward a science
of VLSI design"



- Head-in-sand attitudes

Outline

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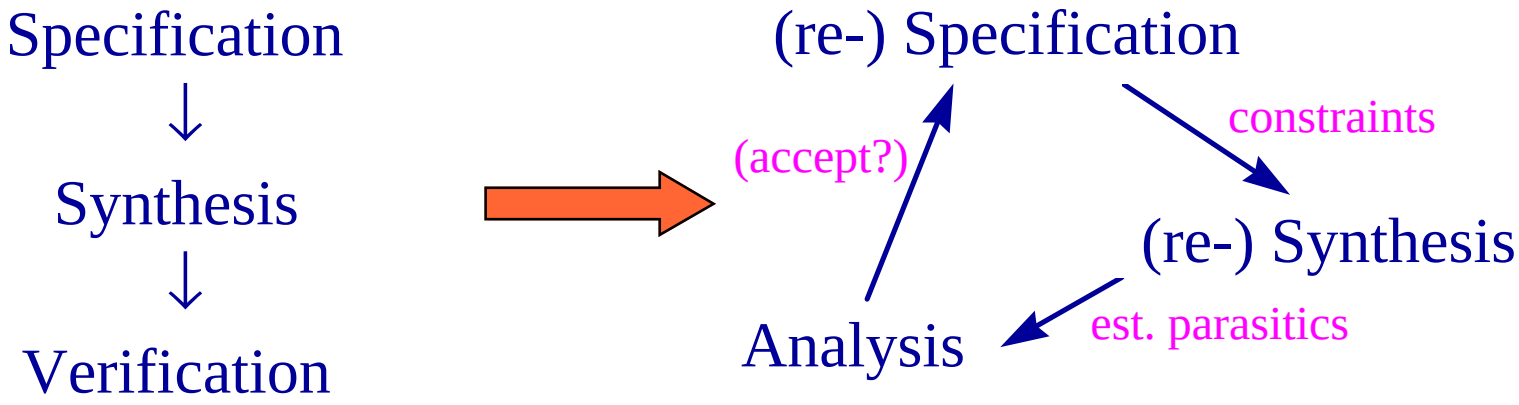
Mindset Change

- "Flow-internal hooks"
- Use all available information at all times
  - simulation traces → activity factors/windows
  - clock phases, offsets
  - hierarchy block names, depths
  - sensitivity analyses
- ⟹ "Cheat whenever possible"
- Side effect = unifications
  - technology mapping ⟺ layout synthesis
  - timing, clock, test synthesis ⟺ placement
  - placement ⟺ routing

Mindset Change

- Methodology … will only go so far
  - correct by construction → construct by correction
  - analysis backplane : close analysis-synthesis loops



- ⟹ Support <u>incremental</u> design and <u>partial</u> design

Mindset Change

- Modeling / estimation : a core competency
  - enables forward synthesis
- Must model both instances and tools
  - which knobs matter ?
  - tool scaling, size/runtime/quality tradeoff profile
  - parameterize, collect design data points
- Example: TDD of TDD (!)

R&D Portfolio: Do or Die

- Commodity analyses (DC, RCX, power, …)
- Commodity data models, interfaces
- Flow-internal hooks, unifications
- Modeling / estimation technology
- Technology context awareness

Technology Awareness Example

- What does a high-performance µP or ASIC look like ?
  - M_{local} w,h,p,t 130 312 260 320
  - $M_{semi\text{-}g}$ w,h,p,t - - 600 -
  - M_{global} w,h,p,t - - 4000 -
  - $area_{die}$ $area_{logic}$ V_{dd} pwr #ML $\#xtor_{logic}$ 5.2cm^2 1.1cm^2 1.2V 135W 8 3.6e+07
  - NAND (FO=3) L_{eff} t_{ox} t_{davg} 50nm 1.8nm 23ps
  - $L_{net\text{-}logic}$ L_{edge} RC_{M1} $RC_{2\mu mgl}$ 78 22800 5400 0.77 ; 55 0.72 (Ω/cm pF/cm)
  - t_{dedge} t_{dgates} (D=12) t_{dcycle} freq 175ps 275ps 450ps 2000MHz
- Structure: DP pipelined superscalar vliw vector memory I/O ...

R&D Portfolio: Bets

- Statistical design !
- Deep understanding of process roadmap implications
- Symmetric multiprocessing (corollary: NT)
- Global optimization as core competency
- Device-level layout synthesis

Conclusions

- Challenging business and technology contexts
- Futures = Consolidations + Unifications
  - syntheses and analyses
  - objectives and optimizations
  - logical and physical
  - temporal and spatial
  - disparate disciplines → the "science of VLSI design"
  - industry and academia

Benjamin Franklin

We must hang together, or else we will surely hang separately.