Design Implementation Mechanisms for PPAC Extension in Late and Mature CMOS Technology

Andrew B. Kahng
UCSD CSE and ECE Departments

abk@ucsd.edu
http://vlsicad.ucsd.edu
Two Megatrends

• **Race to the End of the Roadmap**
  • Technology and design enablement: go big or go home
  • Node pacing not slowing despite near-term “red bricks”
    • EUV, Cu replacement, reliability, layout restrictions, …
  • Mismatch of design-process time constants $\rightarrow$ margins!
    • Root cause of model-hardware miscorrelation, model guardbands
  • Paper to v1.0 SPICE models: 18 months $\rightarrow$ 12 months @N10

• **Low-Power Grand Challenge**
  • Critical for all drivers: mobility, big data, cloud, IoT
  • Design complexity: system + analysis + optimization
    • Multiple supply voltages
    • Extreme power, clock gating
    • DVFS, MTCMOS, Multi-Lgate, …
Design Closure Careabouts

- Temp inversion
- Noise
- MCMM
- Maxtrans
- PBA
- EM
- AOCV / POCV
- Dynamic IR
- Fixed-margin spec
- Phys-aware timing ECO
- Multi-patterning
- Mis
- Cell-POCV
- Min implant
- MOL, BEOL R
- LVF
- BTI
- BEOL, MOL variations
- Signoff criteria with AVS
- SOC complexity
- Fill effects
- Layout rules

A. B. Kahng, SRC Summer Study 150623
FinFET: Drive, Body Effect, Discreteness

- Better electrostatic control + continued gate length scaling
  - Drive current $\uparrow \Rightarrow$ cell height $\downarrow$ (e.g., 8.25T), better area density (w/ fin height $\uparrow$)
  - Effective width $\approx 1.6x$ equivalent area with planar devices
- Current density $\uparrow$, body effect $\downarrow$, fin discreteness $\Rightarrow$ ???

Corner Explosion

**Operating modes**: nominal, turbo, LP1, LP2 …

**FE corners**: FF, FFG, FS, SF, TT, SSG, SS …

**BE corners**: C-worst, Cc-worst, RC-best …

**Temp corners**: temperature inversion corners …

**Split corners**: memory, logic rails with synch interfaces
Design-Based Mechanisms for PPAC Scaling

- Adaptivity
- Signoff Criteria
- Model-Hardware Correlation
- Recovery of “Free” Margin
- Physical Design
- Optimization

Message: design-based mechanisms can unlock nodes of PPAC scaling value!
## Low-Power Design Technology Roadmap

### Introduced in 2011 ITRS Design Chapter

<table>
<thead>
<tr>
<th>Design Technology Improvement</th>
<th>Year</th>
<th>Improvements</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Dynamic</td>
<td>Static</td>
</tr>
<tr>
<td>Low Power Physical Libraries</td>
<td>Before 2011</td>
<td>1.50</td>
<td>1.50</td>
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<tr>
<td>Back Biasing</td>
<td></td>
<td>1.00</td>
<td>1.35</td>
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<tr>
<td>Adaptive Body Biasing (ABB)</td>
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<td>1.20</td>
<td>2.00</td>
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<tr>
<td>Power Gating</td>
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<td>0.90</td>
<td>10.00</td>
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<td>Dynamic Voltage/Frequency Scaling (DVFS)</td>
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<td>1.50</td>
<td>1.00</td>
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<td>Multilevel Cache Architecture</td>
<td></td>
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<td>1.20</td>
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<tr>
<td>Hardware Multithreading</td>
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<td>1.30</td>
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<tr>
<td>Hardware Virtualization</td>
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<td>1.00</td>
<td>1.20</td>
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<td>Superscalar Architecture</td>
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<td>Symmetric Multiple Processing (SMP)</td>
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<td>Software Virtual Prototype</td>
<td>2011</td>
<td>1.23</td>
<td>1.20</td>
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<td>Frequency Islands</td>
<td>2013</td>
<td>1.26</td>
<td>1.00</td>
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<td>Near-Threshold Computing</td>
<td>2015</td>
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<td>Hardware/Software Co-Partitioning</td>
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<td>Heterogeneous Parallel Processing (AMP)</td>
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<td>1.18</td>
<td>1.00</td>
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<td>Many Core Software Development Tools</td>
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<td>1.20</td>
<td>1.00</td>
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<tr>
<td>Power-Aware Software</td>
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<td>1.21</td>
<td>1.00</td>
</tr>
<tr>
<td>Asynchronous Design</td>
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<td>1.21</td>
<td>1.00</td>
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<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>4.66</strong></td>
<td><strong>0.96</strong></td>
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</table>
ADDED in 2013 Roadmap

Approximate Computing
• Variable-accuracy computing (e.g., flexibly from 64b ↔ 16b)

4D Computing
• Reconfiguration on the fly

Adaptivity
• Recapture overdesign from wearout, variation margins

Power Gating Replacement
• HVT device as power switch hits headroom, area wall → ?

Extreme Heterogeneity
• “coprocessor-dominated architectures”
  • (pervasive heterogeneity; energy-efficiency from specialization; HW accelerators)

Extreme Power Gating
• Reaching the limits of shut-off

Signoff At Typical
• Use adaptivity to recover margin, overdesign
Design-Based Mechanisms for PPAC Scaling

- **Adaptivity**
  - Adaptive Voltage Scaling (AVS)
  - Recover dynamic power from overdesign
  - Enable “signoff at typical”, etc.

- **Signoff Criteria**
- Model-Hardware Correlation
- Recovery of “Free” Margin
- Physical Design
- Optimization
Adaptive Voltage Scaling

**Power**

- **Open Loop AVS**
  - Freq. & $V_{dd}$ LUT
  - Post-silicon characterization

- **Closed-Loop AVS**
  - Generic monitor
  - Design dependent replica
  - In-situ monitor

- **Error Detection System**

- **Application Driven AVS**
  - Load-aware AVS (software technique)

**AVS**
- Pre-characterize LUT [Martin02]

**Process-aware AVS**
- Post-silicon characterization [Tschanz03]

**Process and temperature-aware AVS**
- Generic on-chip monitor [Burd00]
- Design-dependent monitor [Elgebaly07, Drake08, Chan12]
- In-situ performance monitor
  - Measure actual critical paths [Hartman06, Fick10]
  - Error detection and correction system
  - $V_{dd}$ scaling until error occurs [Das06, Tschanz10]

**Loading-aware AVS**
- Application-driven $V_{dd}$ and frequency scaling [Lin09]
“Process-aware Voltage Scaling” (PVS) [ICCAD-2012]

- Monitor design considerations
  - Critical path hard to identify (3rd party IP)
  - Multiple modes/voltages: $F_{\text{max}}$ calibration requires long test time

- UCSD: generic, tunable monitor
  - RO-based monitor with $V_{\text{min,ro}} > V_{\text{min}}$ for any data path at any process condition (generic $\Leftrightarrow$ overdesign)
  - Monitor is tunable based on $F_{\text{max}}$ of sample chips to recover design margin (calibrate once)

- Abstracts voltage scaling property instead of matching critical path

- Google: “PVS Snapdragon” 😊
Design-Based Mechanisms for PPAC Scaling

- Adaptivity
- **Signoff Criteria**
  - Signoff blocks tapeout
  - “Who owns the scrap?” business issue
  - Many layers of conservatism
- Model-Hardware Correlation
- Recovery of “Free” Margin
- Physical Design
- Optimization
I. Tightened BEOL Corners ("TBC")

Conventional Signoff

- Routed design
- Timing analysis using conventional BEOL corners (CBC)
  - ECO using CBC
  - violation = 0?
    - No: done
    - Yes: ECO using TBC

UCSD, 2014

- Routed design
- Classify timing critical paths
  - $G_{TBC}$
  - $G_{CBC}$
  - Timing analysis using TBC
    - violation = 0?
      - No: ECO using TBC
      - Yes: done
  - Timing analysis using CBC
    - violation = 0?
      - No: ECO using CBC
      - Yes: done
Practical Filter for TBC-Amenable Paths

-3σ_j  3σ_j  d_j(Y_{CBC}) - d_j(Y_{typ})  Large pessimism  delay

Δd(Y_{rcw})/d(Y_{typ})

Δd(Y_{cw})/d(Y_{typ})
Benefits of Tightened BEOL Corners

- **WNS** and **TNS** are reduced by up to **100ps** and **53ns**
  - #Timing violations reduced by **24% to 100%** [Moore’s Law: 1% / week !]
  - **TBC-0.6**: more benefits
  - Tradeoff between reduced margin vs. #paths which use TBC

- **In production now 😊**
II. Better Signoff Definition (AVS + Aging)

- $V_{\text{BTI}}$: Voltage for BTI-aging estimation
- $V_{\text{lib}}$: Supply voltage for timing library characterization
- $V_{\text{final}}$: $V_{\text{dd}}$ of a circuit with AVS at end-of-lifetime

[Diagram]

- $V_{\text{BTI}}$ and $V_{\text{lib}}$ depend on aging during AVS ($V_{\text{final}}$)
- $V_{\text{final}}$ depends on circuit
- Chicken & Egg Loop

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“Knee” Point for Signoff Definition

<table>
<thead>
<tr>
<th>Low $V_{\text{lib}}$</th>
<th>High $V_{\text{lib}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low $V_{\text{BTI}}$</td>
<td>Slower circuit</td>
</tr>
<tr>
<td></td>
<td>Less aging</td>
</tr>
<tr>
<td></td>
<td>Faster circuit</td>
</tr>
<tr>
<td></td>
<td>Less aging</td>
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<tr>
<td>High $V_{\text{BTI}}$</td>
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<td></td>
<td>More aging</td>
</tr>
<tr>
<td></td>
<td>Faster circuit</td>
</tr>
<tr>
<td></td>
<td>More aging</td>
</tr>
</tbody>
</table>

Optimistic aging library \(\rightarrow\) large power penalty

Overly pessimistic aging library \(\rightarrow\) large area penalty

Our method finds “Knee” point for balanced area and power tradeoff

Experiment setup:
DC/AC BTI @ 125°C
32nm PTM technology
4 benchmark circuit implementations
Design-Based Mechanisms for PPAC Scaling

• Adaptivity
• Signoff Criteria
• **Model-Hardware Correlation**
  • Modeling standards
  • Analysis flows (“closing loops”)
• Recovery of “Free” Margin
• Physical Design
• Optimization
Improved Variation Models Always Welcome

• Monte Carlo path delay simulation shows asymmetric path delay distribution under process variation → Need separate $\sigma$ values for setup and hold analysis
• LVF (Liberty Variation Format) can handle such non-Gaussian distribution; not arriving until N10 or below
• Next: BEOL; partial reversion to gba from pba; …

(from [Rithe et al.])

Liberty Variation Format (LVF) shows reduced pessimism
And, Close Analysis Loops!
And, Close Analysis Loops!
Example Pessimism Reduction Benefit

- Dynamic Voltage Drop: awareness of instantaneous signal transitions around clock edges
- Signal timing windows (TW) from STA model instantaneous transitions
- Iterate TW update, DVD analysis to reduce timing slack pessimism

Initial DVD IR drop map (Tool = Apache Redhawk)
(peak drop = 170mV (rail-to-rail), nominal VDD = 0.9V)

Design = Extracted logic and memories from THEIA (OpenCore GPU)
Tech = 28nm FDSOI
Clock period = 3.4ns

Slacks converge after the 4th iteration due to more accurate estimation of signal slews (IR drop slows down the transitions)

The iterations remove timing pessimism (> 100ps)
Design-Based Mechanisms for PPAC Scaling

- Adaptivity
- Signoff Criteria
- Model-Hardware Correlation
- **Recovery of “Free” Margin**
- Physical Design
- Optimization
Flexible FF Timing $\rightarrow$ Margin Recovery

- Setup time, hold time and clock-to-q (c2q) delay of FF
  $\Rightarrow$ values interdependent, but NOT fixed
- Flexible FF timing model can exploit operating (function/test) modes
  $\Rightarrow$ “Free” pessimism reduction in STA

**Goal:** Find best \{setup, hold, c2q\} for each FF instance

- Sequential LP:
  - setup-c2q opt
  - hold-c2q opt
Improved Timing Signoff Flow

Netlist (and SPEF, if routed)

Extract path timing information

LP formulation with flexible flip-flop timing model

Solve Sequential LP $(STA_{FT_{max}}, STA_{FT_{min}})$

Solution

Annotate new timing model for each flip-flop

Timing signoff with annotated timing

Takeaways

- Fix timing violations “for free”
- 48ps average slack improvement over 5 designs in foundry 65nm technology

Next

- Better exploitation of disjoint cycles/modes
- More accurate modeling of setup-hold-c2q tradeoff
- Circuit optimization should natively exploit FF timing model flexibility
- + cycle-to-cycle jitter margin + …
Design-Based Mechanisms for PPAC Scaling

• Adaptivity
• Signoff Criteria
• Model-Hardware Correlation
• Recovery of “Free” Margin
• Physical Design
• Optimization
I. Placement-Sizing Interference

- New “interferences” between post-layout optimization and P&R
- Rules for device layers (FEOL) become considerably more complex and restrictive
  - Minimum implant width rules for implant region
  - Minimum notch and jog width rule for oxide diffusion (OD)
- Correct (composable) by construction is too expensive!

[GLSVLSI14][ICCAD15]
Lose Correctness By Construction!

- Drain-to-drain abutment (DDA)

- Example solution

"Construct by Correction" removes composability cost, but interlocks the layout and sizing optimizations.

[GLSVLSI14][ICCAD15]
II. Design Automation-Technology Co-Opt

- Patterning choice $\rightarrow$ design rules $\rightarrow$ chip QoR

**Option 1**
Self-aligned double patterning (SADP)
- Small metal pitch
- 7.5T standard cells

**Option 2**
Litho-etch-litho-etch (LELE)
- Large metal pitch
- 9T standard cells

Will option 1 win?
$\rightarrow$ Not necessarily

MinOverlap $<$ MinSpacing

Impact of patterning choice-induced design rules on chip QoR is unclear

Early evaluation of design rules is important for patterning choice!

Pin access problem
OptRouter: Sub-20nm BEOL Rule Evaluation

Routing Clips
Routing Rules Options 1, 2, ..

OptRouter
Generate Routing Graphs
ILP Formulation
ILP Solver (CPLEX)

Routing cost of each rule
III. Design-Tech Co-Optimization = Soft Landings

• Traditional interconnect: aspect ratio (AR) $\approx 2$, linewidth-pitch duty cycle (DC) $\approx 0.5$.
• Intel 14nm BEOL stack (M1 pitch = 52nm): lower AR, higher DC
  why ???
• **UCSD work:** BEOL stack scaling for advanced CMOS technology nodes
  • {lower AR, higher DC} can achieve better performance, EDP
  • Softer landing (12nm trench CD limit) for Mx layers in N7, N6, N5 nodes?

<table>
<thead>
<tr>
<th>Tech. node</th>
<th>M1 T_{def}</th>
<th>AR</th>
<th>DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>22nm</td>
<td>80nm</td>
<td>2.35~2.1</td>
<td>0.42~0.47</td>
</tr>
<tr>
<td>14nm</td>
<td>55nm</td>
<td>1.9~1.82</td>
<td>0.55~0.57</td>
</tr>
<tr>
<td>10nm</td>
<td>46nm</td>
<td>1.68~1.51</td>
<td>0.65~0.72</td>
</tr>
<tr>
<td>7nm</td>
<td>40nm</td>
<td>1.71~1.53</td>
<td>0.65~0.72</td>
</tr>
</tbody>
</table>

Intel 14nm Interconnect stack

Iso-EDP AR and DC choices (pitch = 52nm)
IV. Mixed Cell Height Implementation (!)

- Large cell height $\rightarrow$ better timing, but large area and power
- Small cell height $\rightarrow$ smaller area/power per gate, but large delay and more #buffers
- **Mixing cell height enables tradeoffs between performance and area/power (recall FinFET!) $\rightarrow$ better design QoR**
  - E.g., use large-height high-fanin cells to improve pin accessibility
  - Already have flop trays, etc. as problematic multi-height instances

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**Technology: 28nm LP**

**RED:** 12T cells = larger area, smaller delay

**BLUE:** 8T cells = smaller area, larger delay
Cost of Mixing Cell Heights

- “Breaker cells” required to align regions with different cell heights
  → Optimization must comprehend corresponding area cost

**Diagram:**
- 8T Cell
- 12T Cell
- Assumption: M2 pitch = 64 nm
- Y directional shift:
  - One M2 pitch
- X directional shift:
  - Four sites
- No routing blockage
- Routing blockage on M1/M2

*Assume: M2 pitch = 64 nm*
Optimization Flow

Initial placement
(8T/12T cells “freely” placed)

Partitioning
(Yellow blocks = regions)

Legalization

Technology: 28nm LP
Design: AES
BLUE: 8T cells
RED: 12T cells

Mixed-height placement

New floorplan
Benefits from Mixing Cell Heights

- Technology: 28nm LP (12T/8T)  Design: AES
- 25% area reduction as compared to 12T-only design
- 20% performance improvement compared to 8T-only design
- A current project in my group: “Ultimate 28nm” 😊

![Graph showing area vs. frequency for 12T, 8T, and mixed designs with 25% area reduction and 20% performance improvement.](image)
Design-Based Mechanisms for PPAC Scaling

- Adaptivity
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**Optimization**
- Moore’s Law: 1% per week (however you can get it)
- Get better solutions
- Get them faster
“Big Data” and Machine Learning Applications

**ORION3.0:** A Power-Performance Simulator for Interconnection Networks

**CACTI-IO:** Off-Chip Modeling, Design-Space Exploration

Prediction of maximum bandwidth for the 3D interconnect given a max power, area constraints and clock synchronization scheme.

Optimal clocking scheme for max BW.

**Max BW (GB/s)**

**Max Power Constraint (mW)**

**Max Area Constraint (mm²)**

- **Synchronous**
- **Source-synchronous**
- **Asynchronous**
Pure Optimization for Design Productivity

- Project planning and management are challenging
  - Unforeseen events (late RTL bugs, timing ECO)
  - Resource co-constraints (e.g., two cores per one EDA tool license, three concurrent tapeouts in design center)
- Decision-making is manual, subjective and suboptimal

• How to pack 14 tapeouts into my design center during 2H15?
• Schedule cost minimization (SCM)
  - Minimize overall project makespan subject to delay penalties, resource bounds, resource co-constraints, etc.
• Resource cost minimization (RCM)
  - Minimizes number of resources required across all projects
Example Solver Use Cases (from a design center of a world top-5 semi)

- Schedule modification after a late-breaking design bug
  - Three projects, 11 activities/project (e.g., placement, routing, RCX, STA, etc.)
  - Five resource types (#cores, #memory, licenses for P&R, RCX, STA, tools)
  - Industry solution: Makespan of 41 days across all projects
  - SCM solution: Makespan of 34 days across all projects (1.4 weeks saved)

- Forecast-tethered resource allocation
  - 24 projects, five activities (synthesis, P&R, RCX, STA, PV) per project
  - Forecast allocation for #servers in datacenter
  - Industry solution: Purchase 600 additional servers
  - SCM solution: Zero additional servers

- Human resource allocation
  - Four large projects
  - Four types of human resources (synthesis, P&R, verification, STA)
  - RCM solution: ~$5.2M headcount cost savings for company

- MILP solver website with example inputs and format descriptions at http://vlsicad.ucsd.edu/MILP/
TAKEAWAYS
PPAC Extension: A Few Takeaways

- Next-generation optimizers needed for DVFS/MCMM, wide voltage corners, multi-patterning, FinFET discreteness, …
- Moore’s Law value scaling by cloud EDA and pure optimization!
- Next-generation analysis tools/flows (thermal, dynamic IR, wearout, stress = “next loops to close”; also, stackable models)
- Modeling standards and signoff criteria still need help!
- System-level low-power design continues as both (complexity) challenge and (cross-layer) opportunity
- 3DIC will turn the corner for PPAC envelope (“true 3D” needed)
- Approximate computing will also turn the corner (a bit later)
- Active power regains focus → clock power reduction, active leakage cost, design for min V at given throughput
- Question to SRC: Research? Leave on table? Or ???
THANK YOU!