Modern Physical Design: Algorithm Technology Methodology (Part IV)

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Performance Validation Methodology

- Logic design too early for signal integrity problems
- Placement/Global routing best place to achieve timing convergence
- Placement/Global routing best place to achieve noise immunization
- Detail routing is too late to fix all the signal integrity problems
Crosstalk Induced Errors

- Transition on an adjoining signal causes unintended logic transition
- Symptom: chip fails (repeatably) on certain logic operations

Crosstalk Induced Errors

- Timing dependence on crosstalk
  - timing depends on behavior of adjoining signals
  - symptom: timing predictions inaccurate compared to silicon (effect can be large: 3:1 on individual nets)
Effects of Crosstalk: Delay Uncertainty

Thresholds

min  nom  max

Time (ps)

Voltage (V)

Effects of Crosstalk: Delay Uncertainty

Relative Delay vs. Relative Risetime for different coupling percentages

Relative Delay vs. Relative Risetime for different coupling percentages
**Crosstalk Prevention Strategies**

- **Placement phase**
  - don't know adjacencies, layer assignments, or global routes
  - do know net length, est. wire R/C, driver strength, signal slews
  - establish metrics to tell if net is likely to have problems
  - fixes include driver sizing, buffering
- **Global route phase**
  - don't know adjacencies, but have idea of congestion
  - do know layer assignments, better R/C estimates
  - Can apply timing windows
    - only consider signals that can change at the same time
    - data comes from static timing analysis
- **Detailed routing** - detailed analysis and routing ECOs
- **N.B.:** In any case, SI brings potential huge infrastructure changes (e.g., statistical centering design w/distributions)

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**Pre-Route Pruning**

- **Victim Pruning**
  - sensitivity to coupling effects
  - likelihood of being on a critical path (delay analysis only)
- **Aggressor Pruning**
  - drive strength and load
- **Impact Pruning**
  - victim-aggressor pairs
  - physical proximity of net pairs
  - relationship in the time domain
Post-Route Pruning

- Geometric/Capacitive coupling
  - depends on magnitude of coupling capacitance as compared to total capacitance of net
  - Typically less than 10% of nets have significant couplings and couplings to only few nets are significant
- Structural Filtering
  - take into consideration the type of gate driving the nets
  - consider direction of signal propagation or location of driver
  - victim net with weak driver is more likely to have glitch
  - aggressor net with strong driver is more likely to cause glitch on victim nets
- Temporal Pruning
  - switching windows between victim and aggressor nets is used
- Functional or Logical Pruning
  - eliminate signals/paths that can never be responsible for noise
- Finally, need detailed analysis after filtering stage

Timing and Logic Dependence for Glitch

- Structured filtering determines the potentially significant couplings
- Need to tie in the timing or switching window information to determine if indeed these are relevant
- Coupled nets switching at non-overlapping intervals
  - coupling capacitance can be converted to a grounded capacitance
- Coupled nets switch simultaneously with overlapped intervals
  - need to analyze both nets with their drivers simultaneously
  - coupling capacitance can be converted to a grounded capacitance with worst-case switch factor
Reducing Conservatism

- Aggressor nets are not uncorrelated
  - timing correlation: some nodes cannot switch at the same time
  - noise effect depends on switching windows of nets

- Logic correlation: some nodes cannot switch in opposite direction and some nodes switch monotonically in one direction

Criteria for Immunizing Against Crosstalk

- Need models for noise estimation and delay uncertainty computation with tight upper bounds
- Need timing windows and logical transition between coupled nets
- Need physical information
  - accurate estimation of RCs, congestion, density, pin location, and layer information in pre-routing stages
- Fidelity of models is important
**Issues for Delay Uncertainty**

- Parameters that effect victim net’s gate and interconnect delays
  - aggressor net(s) coupling capacitance
  - fast slew time at aggressor nets and large aggressor net drivers
  - slow slew time on victim net and small victim net drivers
  - proximity of aggressor driver to victim net’s driver (same direction vs opposite direction signal propagation)
  - power bounce in victim driver/receiver gates
- Impact the following delay components
  - victim net driver gate delay
  - victim net delay
  - victim net receiver gate delay
**Impact of Coupling on Delay**

- Coupling adds delay ambiguity/uncertainty
  - amount of coupling depends on the temporal relationship between waveforms; coupling varies between nodes of distributed coupled RC networks

- Current timing tools employ a technique which convert coupling caps. to grounded caps by multiplying with a switch factor depending upon switching conditions
  - reduces coupled RC networks to just uncoupled RC networks
  - allows efficient interconnect delay analysis
  - introduces error in delay computation
  - can it be applicable for worst-case analysis?

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**Timing Windows for Crosstalk**

- Only consider signals that can change at the same time
- Data comes from static timing analysis

Worst case occurs here, does not include signals A or D.
Electrical Analysis

- Standard timing: knows only min/max arrival at any node
- Event-based analysis: knows all node activity

Crosstalk Analysis Approaches

- Simple worst case model
  - assume all aggressor nets are switching simultaneously in opposite direction to victim net
  - functional and timing information not considered
  - yields pessimistic results
- Static Analysis Model
  - timing information is used but function information is ignored
  - yields accurate results but might flag too many nets as problematic
Crosstalk Analysis Approaches

- Zero-Delay Model
  - temporal information is ignored
  - search functional space to find input vectors causing maximum noise
  - if both aggressor and victim nets switch in the same cycle then assumes conservatively that transitions are correlated

- Delay-Vector Model
  - consider both timing and functional information completely
  - not always possible to obtain exact vectors causing maximum noise

\[
\begin{align*}
A_1 & \quad \text{A1} \\
V & \\
A_2 & \quad \text{A2}
\end{align*}
\]

Delay-Vector Model

Switch Factor Methodology

- Switch factor for coupling cap. between pair of nets:
  - 0 for nets switching in same direction (in phase)
  - 1 when aggressor net is quiet and only victim net is switching
  - 2 for nets switching in opposite direction (out of phase)

- effective change in voltage, \( \Delta V_{\text{eff}} = V_A - V_B = 2V_{\text{dd}} \)

\[
\begin{align*}
V_A & \\
V_B & \\
C_c & \quad \text{Cc}
\end{align*}
\]

\[
\begin{align*}
A & \quad \text{A} \\
B & \quad \text{B}
\end{align*}
\]

Switch factor depends on slew times, relative offset of waveforms at both nodes

- need accurate models; iterative methods for accurate SF
Standard Practice

- Use SF=2.0 for most coupling nets
  - coupled nets which are part of same logical bus
  - coupled clock nets and regular nets coupling to clock nets
  - pessimistic for some nets and could be optimistic?
  - due to disparity between rise/fall slew times switch factor could be more than 2!
- Switch factor or Miller coefficient (M) for feedback capacitance between gate input and output
  - effective impedance, \( Z_{eff} = \frac{V_A}{s C_c(V_A - V_B)} \sim \frac{1}{SF s C_c} \)
  - SF is a function of transition times and relative delay of signals at A and B

\[
SF = \frac{V_A}{s C_c(V_A - V_B)} \sim \frac{1}{SF s C_c}
\]

Effect of Slew Times on Switch Factor

- SF is in the range (0, 3)
Parameters Affecting Switch Factor

- All possible combinations of switch factors
  \[ SF_{ij} = f (A_j, V_i, T_{ij}, X_{ij}) \]
  - \( A_j \) represents event times for aggressor nets
  - \( V_i \) represents event times for victim net
  - \( T_{ij} \) is ratio of aggressor and victim slew times
  - \( X_{ij} \) is cross-coupling capacitances between aggressor and victim nets
- SF’s depend on events and transition times and vice-versa
  - Hence, requires iterative solution to find accurate SF’s

IR Drop

- Voltage drop in supply lines from currents drawn by cells
- Symptom: chip malfunctions on certain vectors
- Biggest problem: what’s the worst-case vector?

<table>
<thead>
<tr>
<th>Allowable voltage drop at pin</th>
<th>Pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply network consists of wires of varying sizes; they must be big enough, but too big wastes area</td>
<td></td>
</tr>
<tr>
<td>Currents depend on driver type, loads, and how often cell is switched</td>
<td></td>
</tr>
<tr>
<td>Voltages depend on currents of other cells</td>
<td></td>
</tr>
</tbody>
</table>
**IR Drop**

- **Analysis**
  - model I/O P/G supply; C extraction must distinguish decoupling cap between P/G and coupling cap between signals, P/G

- **Prevention (good design)**
  - P/G lines on same layer, close to each other; large decoupling on chip; process solutions (e.g., DEC Alpha)

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**Electromigration**

- Power supply lines fail due to excessive current.
- Symptom: chip eventually fails in the field when wire breaks.

Currents depend on driver type, loads, and how often cell is switched.

Currents depend on currents of other cells.

Current limit depends on wire size.

Power supply network consists of wires of varying sizes; they must be big enough, but too big wastes area.
**Electromigration**

- Prevention: wire cross-section to current rules
- Maximum current density for particular material (via, layer)
- Modified Black's equation; waveform models
- Higher limits for short, thin wires due to grain effects
- Copper: 100x resistance to EM → not a problem any more?

**Hot Electron Effects**

- Also called short-channel effect
- Caused by extremely high electric fields in the channel
  - occurs when voltages are not scaled as fast as dimensions
- Effect becomes worse as devices are turned on harder
- Symptom: thresholds shift over time until chip fails
Hot Electron Prevention Strategies

- Allowable region for input slew and output load
- Fluence per transition is function of input slew, output load
- Set maximum allowed degradation over life of device
  (estimate of total number of transitions) \( \equiv \) fluence limit
- Size device as needed
- Output load vs. driver sizes

Wire Self-Heat

- May also be called signal wire electromigration
- Wire heats above oxide temperature as pulses go through
- Symptom: chip eventually fails when wire breaks
- Depends on metal composition, signal frequency, wire sizes, slew rates, and amount of capacitance driven
- Requires different data/formulas from power supply EM