Some New ECAD Tool Domains & Issues for Design Integrity in the Deep Sub-Micron Era

- **Lithography Process - Optics, Resist, Physical Process**
  - Bitcell Parasitics
  - Post-layout DRC
  - Model-Based Optical Proximity Correction
  - Phase-shift Mask
  - New Rules - avoid phase conflicts

- **Chemical-Mechanical Polish Enhancement (Planarity)**
  - Tiles of Metal in Oxide in Large “Missing Metal” Areas
  - Slots in Wide Metal Busses
  - Rule-based Early Post-layout (Delay Verification Compromised)
  - Pre-layout Rules-based Required

- **Interconnect Modeling**
  - Local, Rules-based
  - Non-local, Inductance, Full EM Calculation
  - Hierarchical
  - Strong Connection Between ALL Levels of Design Hierarchy at High f
New ECAD Tools Will Guarantee Design Integrity in Deep Sub-Micron Era

Old Paradigm - Design -> TCAD
Hierarchy

PRE-Design Calibration (Rules, Models)

Application Synthesis
Virtual Prototyping

HW/SW Partitioning
Architectural Synthesis

Software Synthesis
Compilers
HW/SW Co-verification

Behavioral & Logic Synthesis
Formal & Func. Verification
DFT, DFM, DFD, DFR
Floorplanning, Place&Route
Noise, Power, Delay Extraction
Layout, Parasitics

Virtual Silicon Prototyping
TCAD
Automatic Model Generation
Virtual Package Prototyping
New Process Development

CIM
SPC
Yield Modeling & Synthesis
Reliability Modeling & Syn.
Process Calibration

New Paradigm - Design <-> Technology
Interaction / Iteration
Flow

Behavioral & Logic Synthesis
Formal & Func. Verification
DFT, DFM, DFD, DFR
Floorplanning, Place&Route
Noise, Power, Delay Extraction
Layout, Parasitics

Interconnect Extraction
(Delay Paths, Return Currents, SIV)

OPC / Phase Shift / Optical Process - Induced Shapes “Corruption”

Process Technology “Spurious” Shapes (CMP Tiles, Slotting)

Back Annotation

Post-Layout Design Integrity Tool Suite

Post-Layout Design System

Warren D. Grobman
DigitalDNA from Motorola
New ECAD Tools Will Guarantee Design Integrity in Deep Sub-Micron Era

Old Paradigm - Design -> TCAD Hierarchy

System Definition

Architecture

S/W - Compiler - Verify HW/SW

Synthesis

FloorPlanning

Layout

Specs Verification

TCAD

Virt. Pkg Prototype

New Prod Intro

CIM, SPC

Yield Modeling

Rel. Modeling

Process Calib.

Behavioral & Logic Synthesis

Formal & Func. Verification

DFT, DFM, DFD, DFR

Floorplanning, Place&Route

Noise, Power, Delay Extraction

Layout, Parasitics

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New Paradigm - Design <-> Technology Interaction / Iteration Flow

Flow

PRE - Design Calibration (Rules, Models)

Back Annotation

Post-Layout Design Integrity Tool Suite

Post-Layout Design System

POST - Design

Calibration (Rules, Models)
## Strategic Deep-Submicron ECAD Tools and Systems

<table>
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<tr>
<th>ECAD Tool</th>
<th>DRC</th>
<th>Layout</th>
<th>Parasitics (Delay, Power..)</th>
<th>Front-End Rules</th>
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</thead>
</table>
| Litho Process | Litho Modeling Post-layout | Optical Proximity Layout  
- Rule-based  
- Model-based Phase-Shift |  | ✔️ |
| Chemical / Mechanical Polish | | Tiling / Slotting  
- Rule-based  
- Model-based ("Smart") | Metal Tiles  
- Slots in Metal | ✔️ ✔️ |
| Interconnect | | | Rule-based  
Model-based  
- Local  
- Non-local  
- Hierarchical | |
| Pattern Transfer Process (Etch...) | Post-layout Modeling | ? | ? |
### Status of Deep-Submicron ECAD Tools and Systems

<table>
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**Digital DNA from Motorola**

Design Automation Conference
June 1999

Warren D. Grobman
CMOS Circuit Trends (Schematic)
SIGNAL INTEGRITY ISSUE

Signal wire Cross-sections (Not to scale)

Crosstalk > 3 1/2 X

Require New Simulation Models & Tools
Signal Propagation Regimes
Wafer \( t = 750 \ \mu m \)

- Skin Effect
- TEM
- Slow Wave

Frequency Spectrum for Signal Clocked at 300 MHz

Log (Frequency)

Resistivity \( \Omega \cdot m \)

Bandwidth

300 MHz Clock
Motorola Digital & RF Systems Roadmaps for Gate Length Extend Below Native Stepper Resolution

Stepper Wavelength

Industry Roadmap

Motorola Roadmap

Chart Courtesy of Numerical Technologies, Inc.
Phase Shift Mask & Optical Proximity Correction Software

- Advance Lithographic Dimension
- Best of Breed: IP + Execution
- Extend life of Existing Tools
- Significant Performance Boost
- Lower Cost Die for Embedded Systems
  - Area Advantage (New Design Point)
  - Mfg Tolerance

0.09 micron

AltiVEC PowerPC
>10.5M Transistors
Stepper $\lambda = 0.25$ micron
Phase Shift Greatly Improves Gate Image Definition

Uses phase-modulation at the mask level to further the resolution capabilities of optical lithography

Benefits:

– Smaller feature sizes
– Improved yield (process latitude)
– Dramatically extended useful life of current equipment
– Performance Boost
– Chip Area/Cost Advantage for Embedded Systems

Printed using a ~0.18 \( \mu \text{m} \) nominal process