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Panel Discussion on PSM/OPC Effects: *Influence on Library Development*

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dac1999 innovation

innovation on *fast forward*

Narrow the Focus

- Current discussion only addresses library development at the cell level
  - Intracell routing must be considered
- Constraints on P&R a separate issue
  - Intercell routing outside focus of this presentation

Philosophical Decision

- Throw it all together and fix it after block P&R or chip assembly
  - "Build, test and fix"
- Do it right up front (a/k/a, "correct by construction")
  - Since nobody is perfect, trying to "do it right up front" usually implies some amount of implicit or explicit guardbanding

Build, Test and Fix

- Pushes potential problems closer to tapeout
  - Not a happy option under tapeout pressure
- Test-and-fix of standard cell design at block level breaks the layer of abstraction
  - Breaking the level of abstraction removes the point and value of standard-cell design as a way of managing complexity
    - Timing closure becomes more difficult, along with cell characterization and verification
- Easier to test and fix custom design than standard cell
  - Flow designed up front for such issues

Correct by Construction

- Combinatorics of cell adjacency quickly become unwieldy during the placement phase
  - Problem becomes even more difficult once routing is added
  - Internal cell geometry cannot necessitate fixes outside cell boundary
    - "Rule of Containment"
  - Geometry at edge of cell must be compatible with all potential neighboring cells
    - "Rule of Neighborliness"
      - Phase assignment can't conflict
      - Poly routing at cell edge would probably be bad

Implications & Wild Extrapolations

- OPC/PSM constraints need to be embedded in design rules
  - Not a great option, but better than the alternative
- Std cell design is more constrained ➡ more difficult ➡ higher value-add & cost
- Std cell design becomes incrementally more closely linked to a particular foundry/process
  - Pointer in direction of foundry-specific libraries with royalty model?!
- Loss of area efficiency around cell edges ➡ larger silicon