Question #1

- **Will sub-WL complexity force costly new abstractions? Will we move to lithography simulators inside layout tools?**
  - **Name 3 “rules” or “methodologies” that will be the most effective in keeping process “under the rug”.**

Question #2

- **Is Layout = Silicon really a must ? (Isn't our real goal Functional Design = Realization ?)**
  - **Is there a brave new future world of radically different layout tools, extraction models, circuit design styles ?**
  - **Will this be driven by the mask verification bottleneck ?**

Question #3

- **What are implications of Sub-WL for reuse-based design ?**
  - **cell-based layout and verification, hard-IP reuse ?**
  - **(density control, optics flavors…)**

Question #4

- **Today “ECAD” ends at “GDSII Out”. How will things be different 5 years from now ?**

Question #5

- **So who owns the scrap ? (masks, silicon)**

Question #6

- **Will Sub-WL be a bonanza or a disaster for:**
  - **physical+performance verification and analysis**
  - **custom layout + cell generation tools**
  - **3rd-party hard IP providers**
  - **foundries**
  - **… ?**