How do defects and defect inspection affect you?

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Why defects matter

- Mask turnaround time includes inspection and repair
- Better assured mask quality allows less investment in wafer lithography
- Finding defects early avoids (mysterious) wafer yield busts in prototypes and in production

- One reticle defect can destroy:
  - @ One 50 wafer / hour stepper
  - @ $3500 / wafer cost
- $70,000 / hr
- $1,680,000 / day
- ~ $50 Million / month!
A long time ago, finding defects was difficult but straightforward

- Pinholes and chrome spots
- Opaque particles on quartz
- Edge defects
- Breaks and bridges
Recently, inspectability has become a big deal. But improved inspection tools are catching up to the problem.
Some examples of issues

$D' \neq D'''$

- Design Data $D$
  - Corrections based on $D' > D'''$ model
  - Mask Writer Input $D'$
  - Write Develop Etch
  - Reticle $D''$
  - Mask Inspection System

- Repair
- Expose Develop Etch
- Wafer $D'''$
- Measure

Need 64-bit OS

D'''
Mask Requirements Roadmap

Defect Detection Requirements

Inspection Wavelength
Defect sizes are going down fast

Inspectability limitations on binary masks, such as small geometries (e.g., assist bars) and degenerate geometries (e.g., kissing corners) are becoming non-issues with newer algorithms.
λ/NA dropping fast for inspection sys

Minimum sensitivity (nm)

Year of introduction


100 1000

221L

228

239HR

331/351

353UV

365UV

5xx

Glassen/DAC
On the topic of strong phase shift mask inspection

- Inspection needs to be within one wavelength to see phase shift
- Many popular PSM techniques use two masks per layer. Inspection of these masks are challenging but solvable.
- To minimize defect creation, some mask-makers use “voting” type techniques that require 3 write/develop/etch passes. Killer defects are slightly larger and slightly harder to find--no net win.
Mask Error Factor makes the problem worse, especially for OPC masks

$$MEF = \frac{\Delta CD_{\text{wafer}}}{m \times \Delta CD_{\text{reticle}}}$$

$m = \text{stepper magnification, } (0.20, 0.25)$

For smaller pattern ($k_1 < 0.6$),

reticle errors are amplified.
MEF-Adjusted Mask Specifications

Mask Spec = \frac{\text{Typical Value}}{\text{MEF}}

- CD Uniformity
- Defects

So please help by creating MEF-constrained OPC decoration codes!