Sub-Wavelength Lithography: How Will it Impact Your Design Flow?

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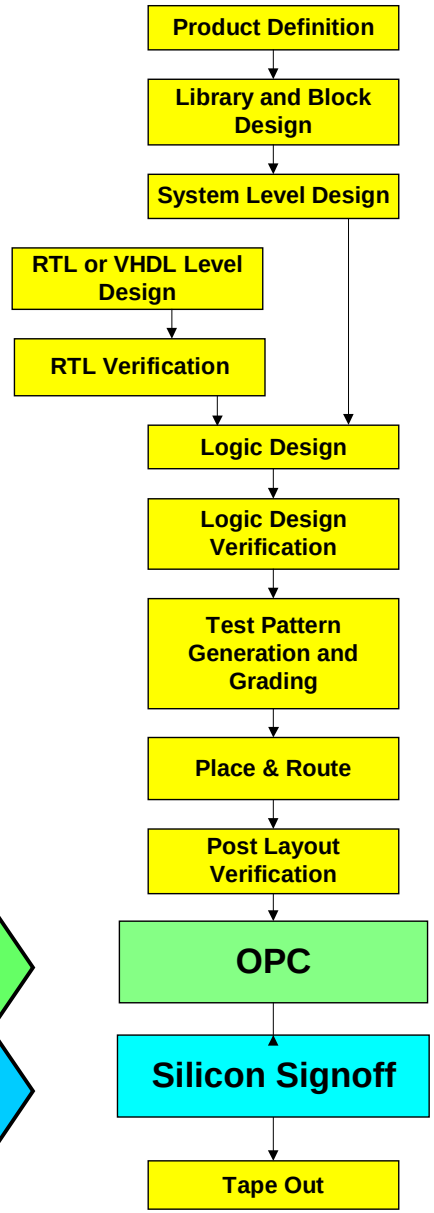
SWL Lithography Demands Design Flow Enhancement

- **Fundamental physics limits conventional printing fidelity and process window**
  - **No 'magic processing bullets' for ~7-10 years min**
- **SWL impact must be mitigated in layout --- *last untapped degree-of-freedom***
  - **All will go through at least some LEM before tapeout**
  - **LEM (Layout Enhancement for Manufacturability) includes: OPC, PSM, & other PPC**
- **Verification tools must both;**
  - **validate generated OPC / PSM features *plus***
  - **account for complex nonlinear residual pattern distortions across process window**
- **Dramatically increasing mask costs / complexity *(> $500k/set ?)/(4x-10x or more ?)* require improved verification before tape-out.**
- **Impact of PSM & OPC spans the entire design flow**
- **Intrinsic complexity/cost of PSM requires comprehensive integrated solution to eliminate long-loop design iterations**

OPC in Today's Design Flow

- Currently implemented post-verification
- Used to compensate conventional binary design *as well as* PSM design
- Rules-based & simulation-based



Currently OPC is Localized

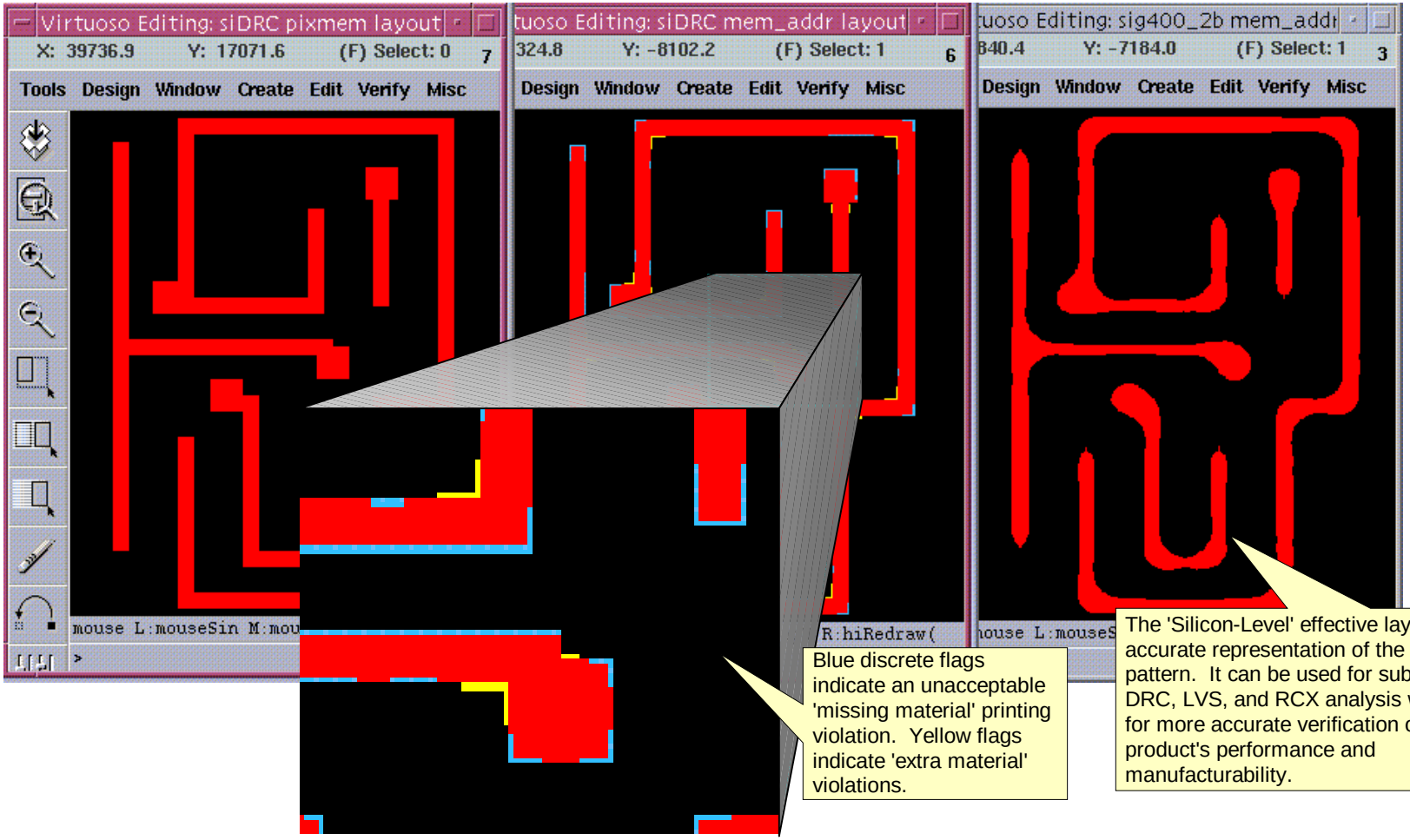
Silicon-Signoff

Silicon-Level Verification

Virtuoso Output of As Designed Layout

Virtuoso Output of NTI Printing Violation Flags

Virtuoso / Assura Output of 'Silicon-Level' Layout

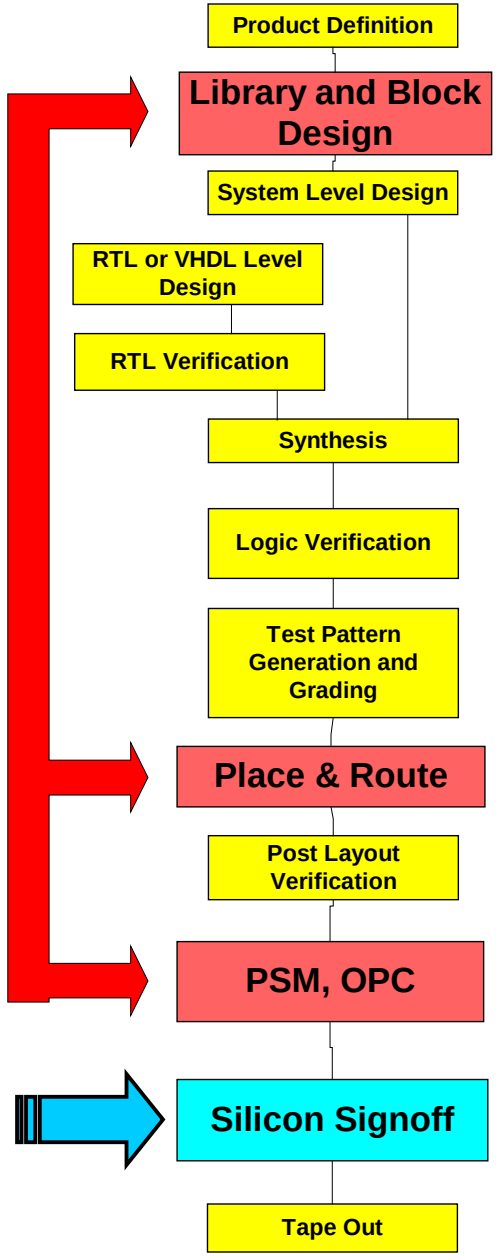


PSM in Today's Design Flow

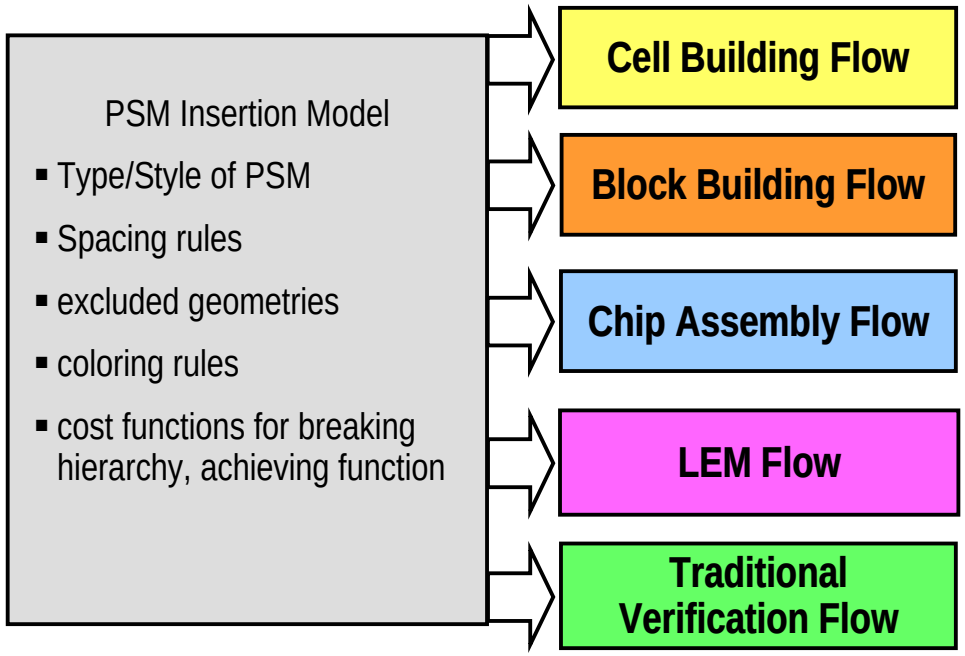
- Limited in scope of application
  - Poly layer only -- performance-driven gate-shrink or memories
  - Not yet area-driven for full-chip / full-block
  - Limited scope allows PSM insertion during layout post-processing
- Automated tools used only in verification space
  - Phase conflict detection
  - Automatic PSM for localized device features (e.g. gates)
  - No automated polygon layout or P&R tools for general logic
- Broader scope requires design tool PSM-awareness

Augmenting the Traditional Flow for PSM

- PSM is disperse & impact is felt throughout the design flow
- PSM / OPC / Si-Verification requires tightly integrated tools
- Upstream design tools need *a-priori* knowledge of downstream insertion model to enable phase-compliant designs
- Downstream insertion tool needs knowledge of any design-level constraints / potentially conflicting activity
- All design flow levels require consistent PSM insertion model -- cell, block, assembly, and verification



PSM Requires Tightly Integrated Design Flows



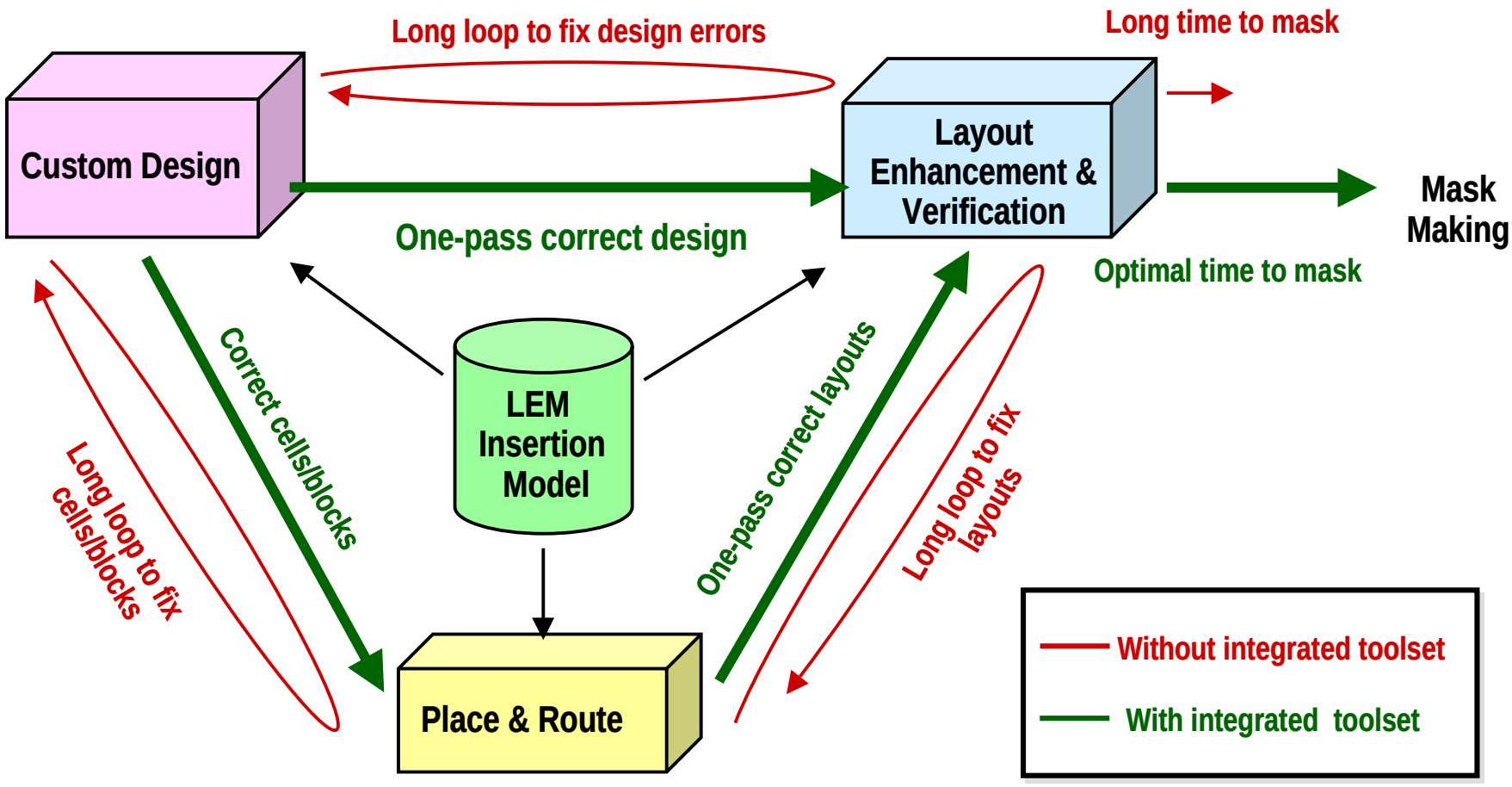
- Phase Compliant Cells
- Phase Compliant Blocks or fully PSM'd and verified blocks
- Phase Compliant Chip or fully PSM'd chip
- PSM'd, OPC'd, and verified design
- Verified LEM elements

Subwavelength Design In an Integrated Environment

Reduced overall design time, cost, & risk

Integration with full-custom and cell-based layout flows

Silicon-Verified Layout



Summary

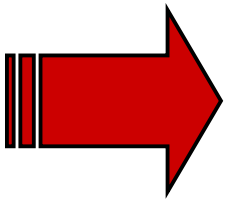
- Design flows to enable PSM, OPC, PPC mask technology require;
  - advanced ‘silicon level’ verification tools for silicon signoff
  - highly integrated design-thru-signoff tools
- SWL problem requires consideration & expertise which span design, verification, advanced mask technology, and lithography physics & the process
- Solutions must be cast in EDA use model
- Tools / flows will handle it --- highly integrated tools and flows are under development in all areas impacted by SWL and DSM process influence

Auxiliary Slides Follow

Will Not be Shown in Regular Presentation

PSM Insertion Point Options

Utilization and management of spatial degrees-of-freedom for PSM insertion model

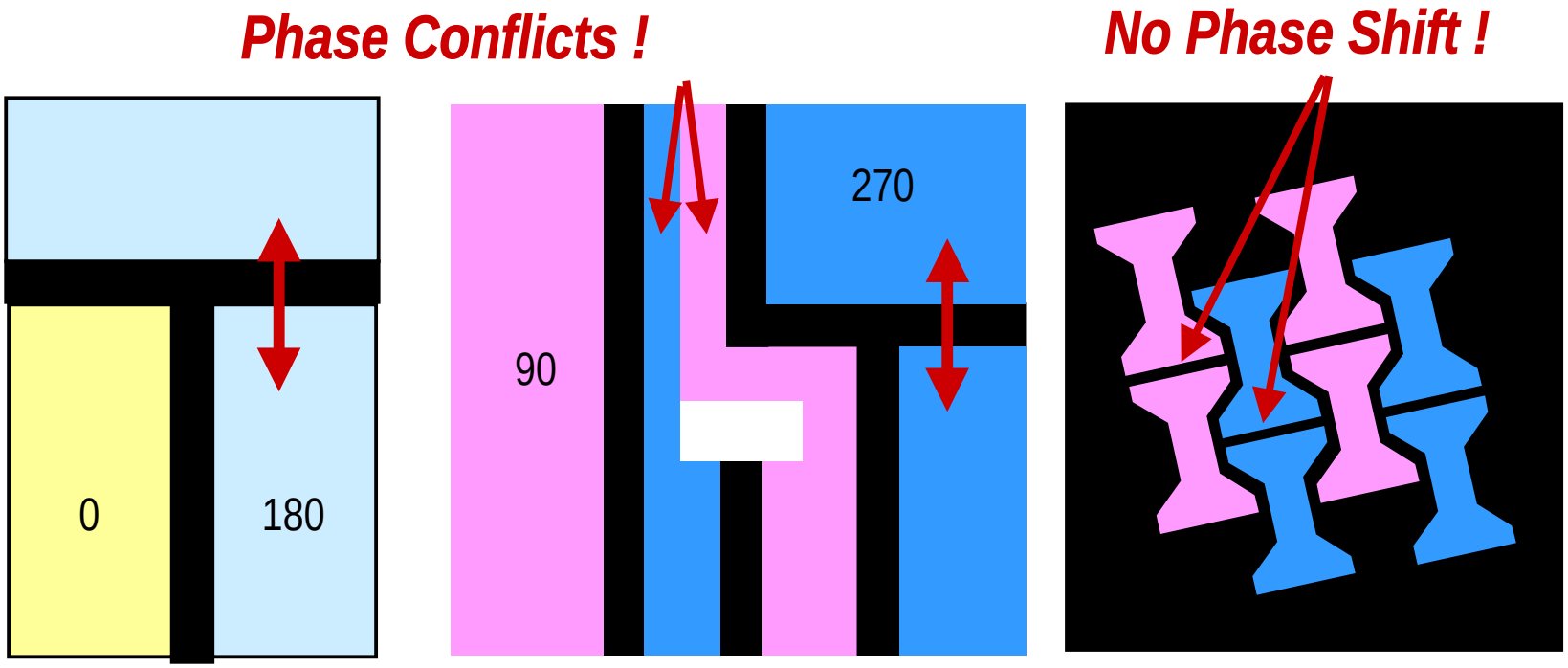


- **PSM -- PSM is done by auto layout tool**
  - All degrees-of-freedom available
- **PSM Compliant Design -- PSM in post-processing but layout is PSM compatible**
  - All needed degrees-of-freedom are available
  - PS assignment is straightforward and quick
- **PSM in post-processing but restrict geometry types/configuration**
  - Minimize unpredictable phase conflicts
  - Speed up post-processing
- **Do PSM as layout post-processing operation -- auto-layout tools unaware of downstream PSM requirements**
  - Complex and time-consuming post-processing
  - Many unpredictable phase-conflicts
  - PSM highly constrained --- usable degrees of freedom are wasted
  - Gets more complex with new generation DR
  - Hiearchy

Sub-Wavelength Era Design-to-Mask Challenges

- Design of advanced subwavelength masks is complex and imposes stringent requirements on tools throughout the entire design flow
- Exponential increases in year-to-year design complexity dictate Moore's Law scalable tool performance and capacity capabilities
- Dramatically increasing costs / complexity of masks expand the application boundary of verification.
- Verification of subwavelength masks creates requirements for new technologies and design flows
- A comprehensive integrated solution is required to eliminate long-loop design iterations in full-custom and cell-based layout flows

Examples of Phase Conflicts



Resolving Phase Conflicts

- Conflicts are resolved by using the available degrees-of-freedom;
  - Expanding poly outside of active area
  - Addition of extra space
  - Selectively not phase shifting certain features
- Layout conflicts cannot be resolved without these required degrees-of-freedom
- Once lost degrees of freedom are very hard retrieve -- long loop cycles are inevitable
- Full custom and cell-based tools must allow required degrees-of-freedom by being PSM-compliant *(aware of excluded geometries, spacing rules, phase-assignment rules…)*