Part 3: Test Structures, Test Chips, In-Line Metrology & Inspection

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Topics

- Introduction to Test Chips
- Test Structures
  - Basic Concepts
  - Problems / Issues
  - Real Wires
- Test Chips
  - Different Functions
- In-Line Structures
  - Metrology
  - Inspection
- Future Design Style Impact on Testchips
- Summary

Introduction to Test Chips

- What are they used for?
  - Technology Development
    - Design Guidelines
      - Spice Models
      - Technology File parameters
      - Design Rules
    - Fab Process Development
      - Unit Processes
      - Process Flow
  - Production monitoring
- Who designs them?
  - Process Integration + Driver-Product Designers
- Who tests / analyzes them?
  - Process Integration + Product Engineering

Test Structures: Basic Concepts

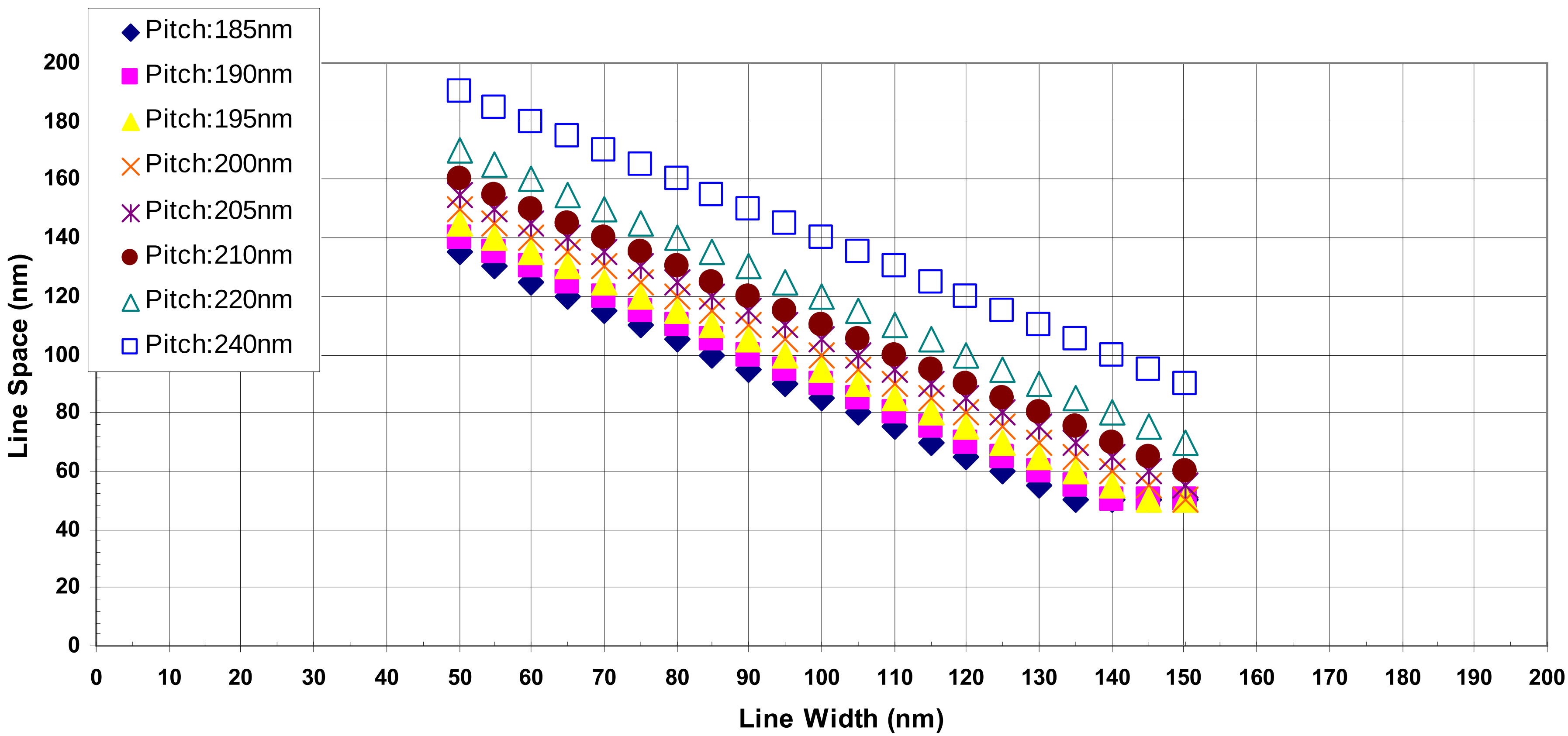
- Partition the device / interconnect
  - What is being tested / stressed?
  - What isn't being tested / stressed?
- Defining the Design Space
  - Focus on the target dimensions for what is being tested, create the space around the target
  - Use relaxed rules for what isn't being tested
- Analyze the results based on the design space DUTs, not just the target DUT

Test Structures: Design Space

- "Design Space" is the Width / Space / Overlap combinations covering what is expected in manufacturing
  - Should cover a region which will show passing results as well as failing results
  - May be limited by patterning capability
- Examples

Test Structures: Design Space Example

- This chip had a design space covering several pitches with many combinations of width and space
- The same combinations were applied to line-width resistors, combs, and comb-serpents



Test Structures: Problems / Issues

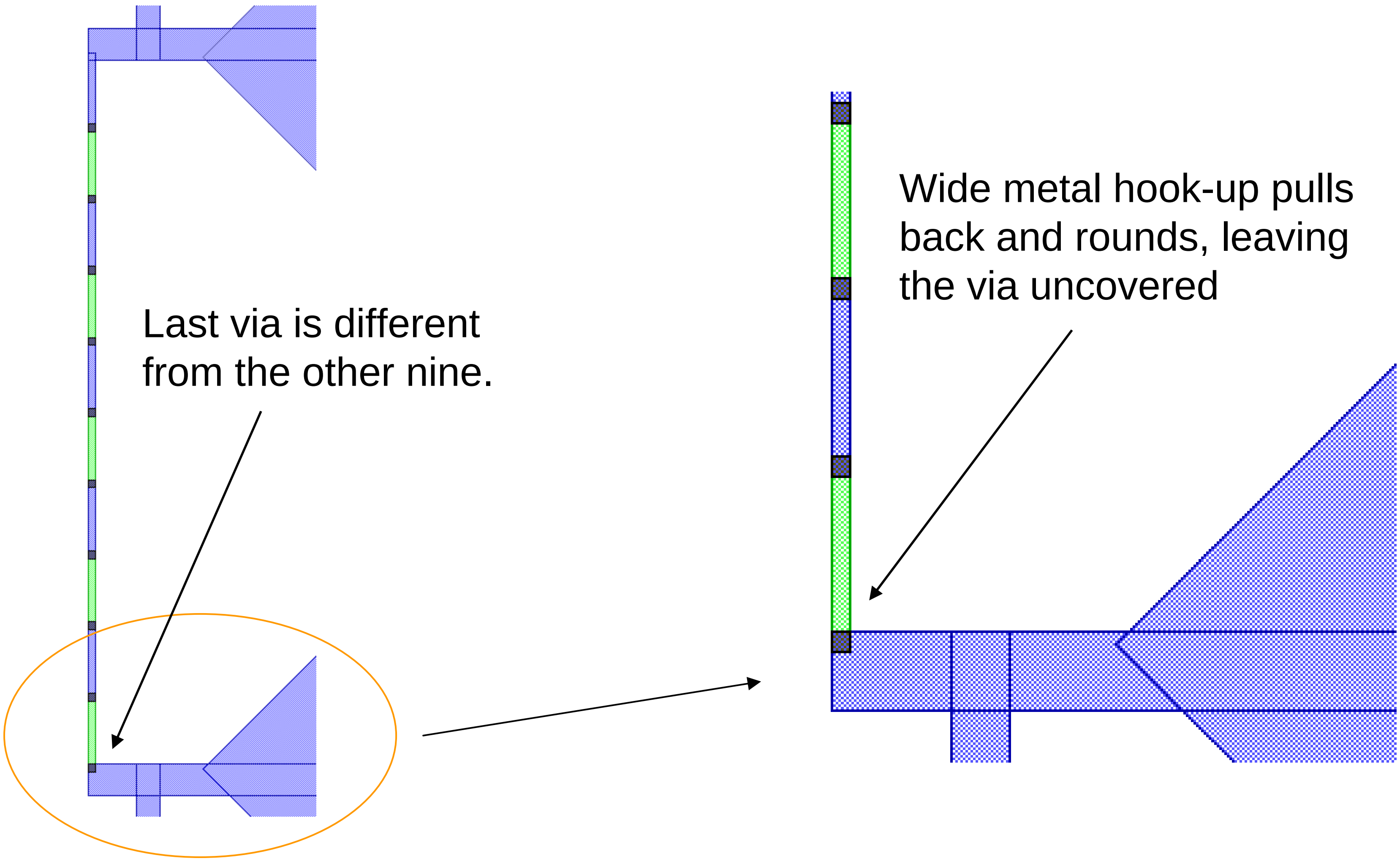
- The root cause of many test structure problems is the failure to “Partition the device / interconnect” Examples
  - Via Chain

- Other problems are caused by just looking at the target device, not the entire design space Examples
  - Line-Width Resistors
  - Comb-Serpents

Test Structure Problem: Via Example

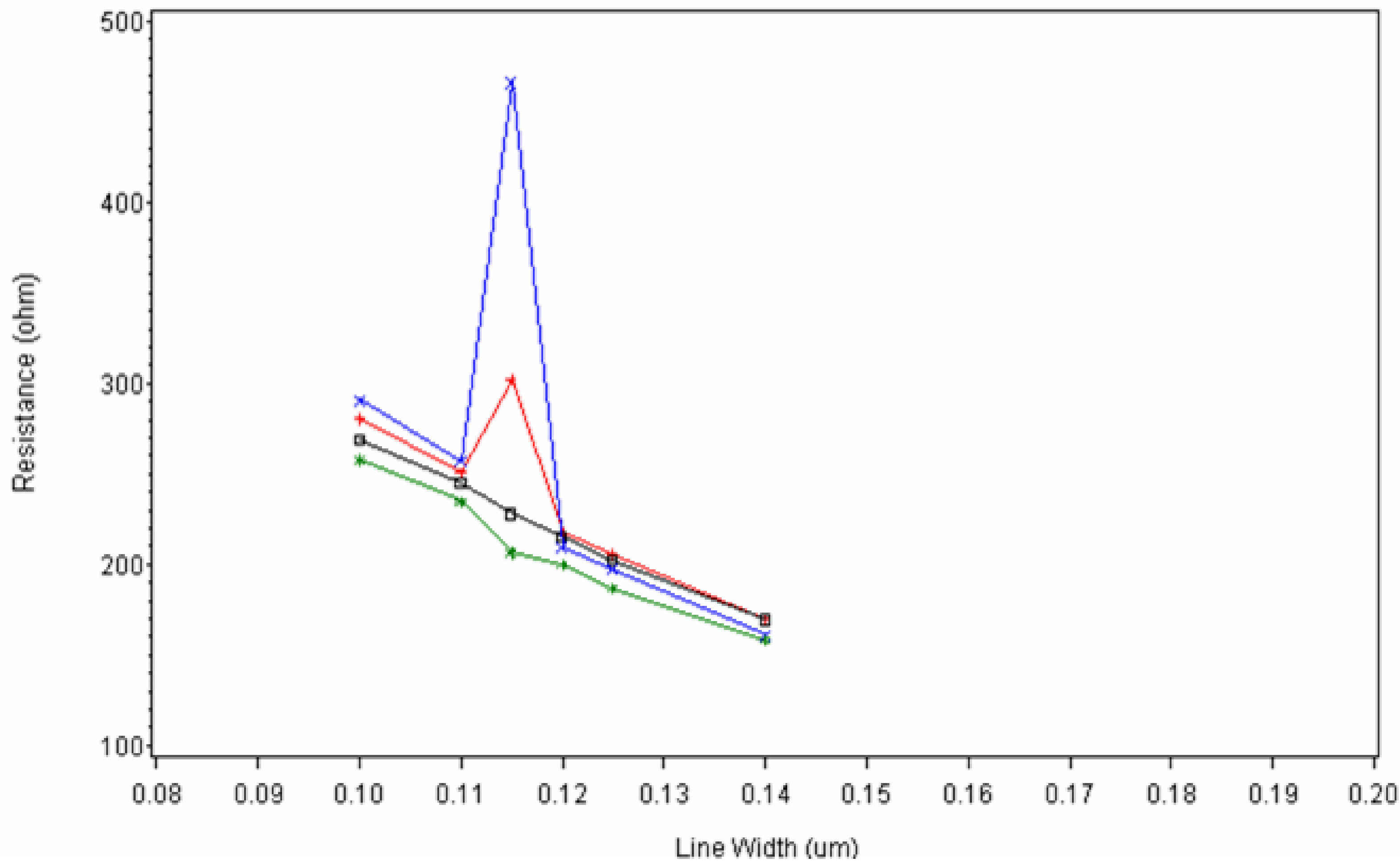
Short Via Chain Hook-up

- Because of the details of the hook-up, this DUT had a high failure rate even though the other vias had good yield



Test Structure Problem: Resistor Example

- Need to look at the entire design space
  - In this case, the 115nm lines in one orientation had an OPC problem; if this had been the target size, with no other DUTs measured, incorrect conclusions would follow



Test Structure Problem: OPC Comparison

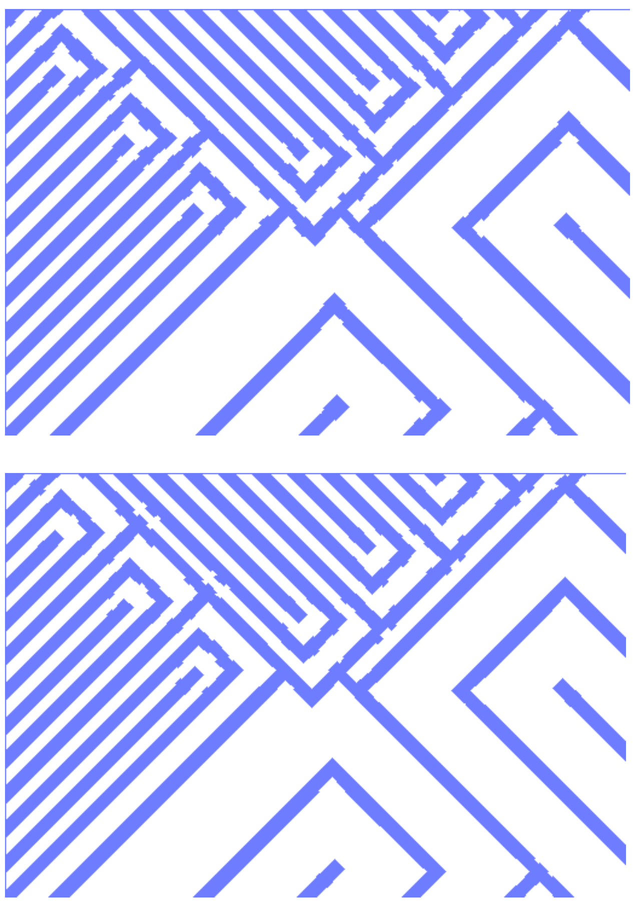
- Comb-Serpent Low Yield at a non-minimum Width/Space
  - KrF OPC was aggressive, ended up with a small space at one pitch
  - ArF OPC required much less layout adjustment, had no problem
  - The issue was found on diagonal structures, but Manhattan DUTs had the same problem

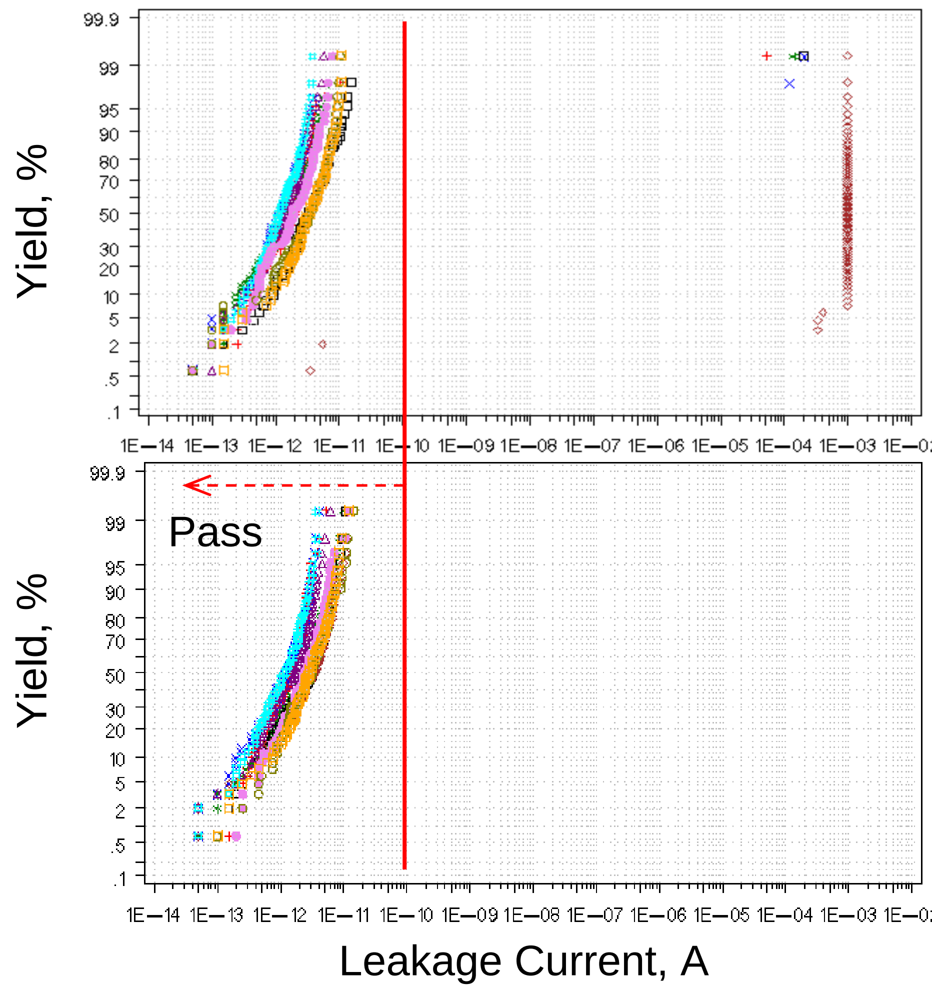
Post-OPC

E-Test

KrF

ArF

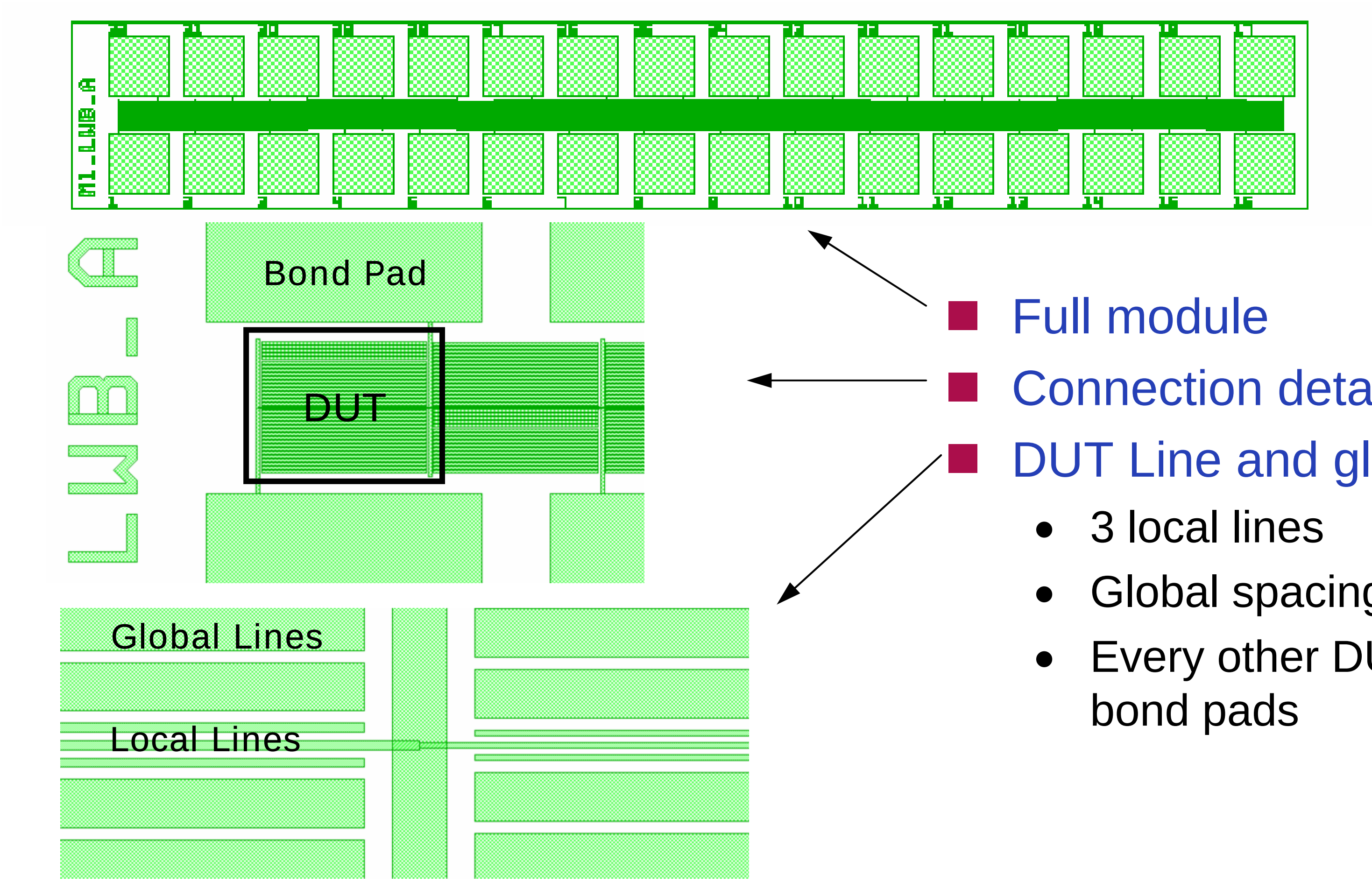




Test Structures: Real Wires

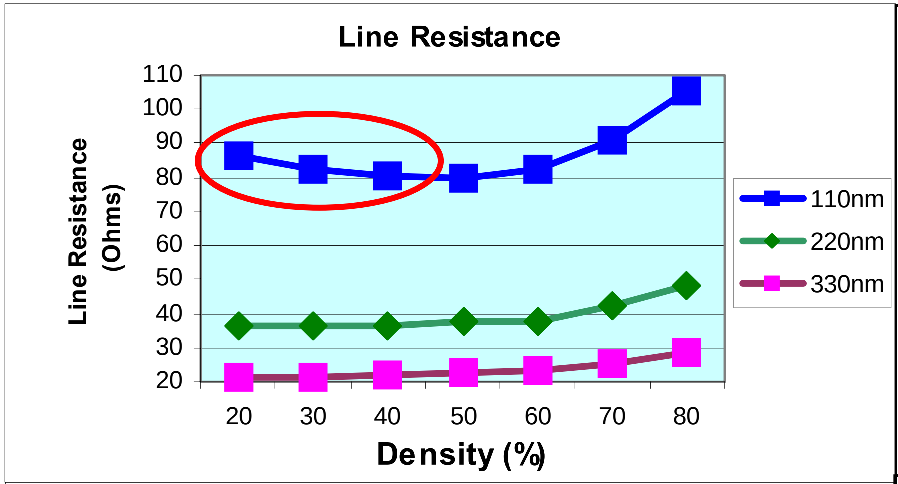
- Many of the structures used on test chips to evaluate copper interconnect look nothing like wires on real chips
- Structures used to evaluate the copper CMP unit process are typically much larger in area and include very wide lines to determine dishing
- Structures used for interconnect modeling should look like “Real Wires”
  - Asymmetric neighborhoods
  - Non-regular local and global lines

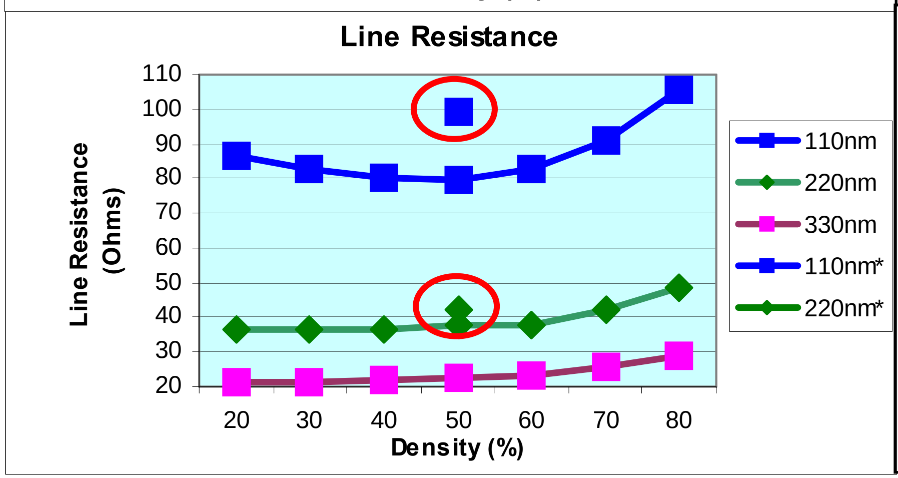
Test Structures: Real Wire Examples



- Full module
- Connection detail
- DUT Line and global line detail
  - 3 local lines
  - Global spacing to local lines
  - Every other DUT adjacent to bond pads

Test Structures: Real Wire Results





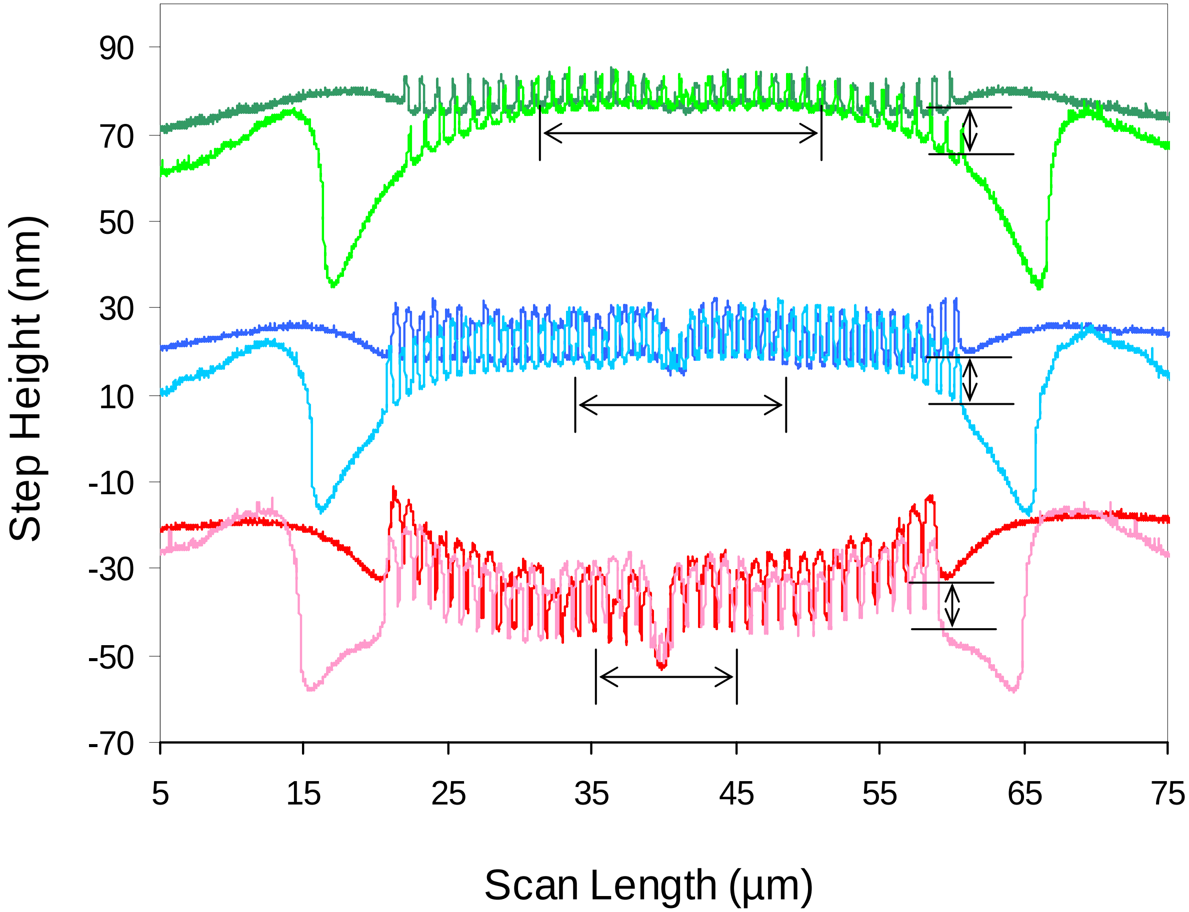
- Dense line results
  - 220, 330nm modeled okay
  - 110nm model not correct
- The need for a new model was clear for 90nm technology

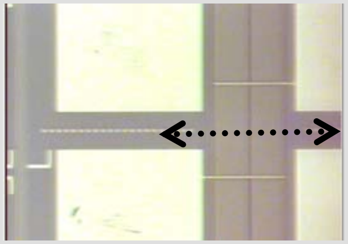
- Global density impact
  - Consistent for a given W/S
  - Different for a different W/S
- Another new model needed to account for global density

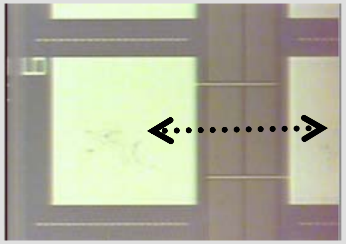
Two interesting results came from these modules:
- Increase in R for 110nm line at 20% density
- Difference in R at a given density depending on global W/S

Test Structures: Real Wire Physical Data

Array Width	40µm	40µm
X-axis N. Distance	> array width	5µm each side

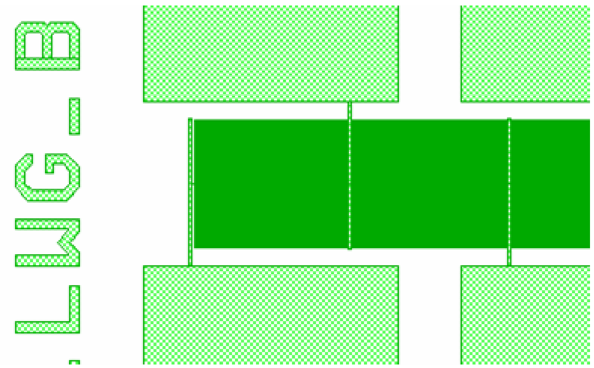




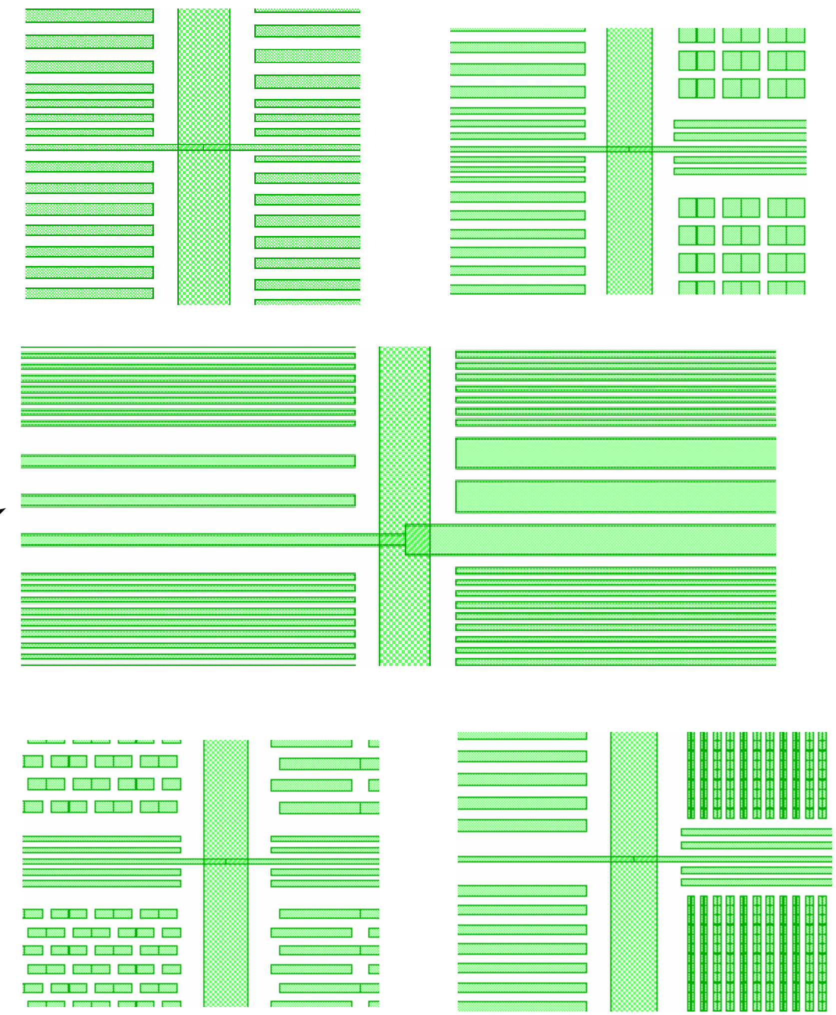


Density	P. Distance
20%	20µm
50%	15µm
80%	10µm

Test Structures: More complex Real Wires

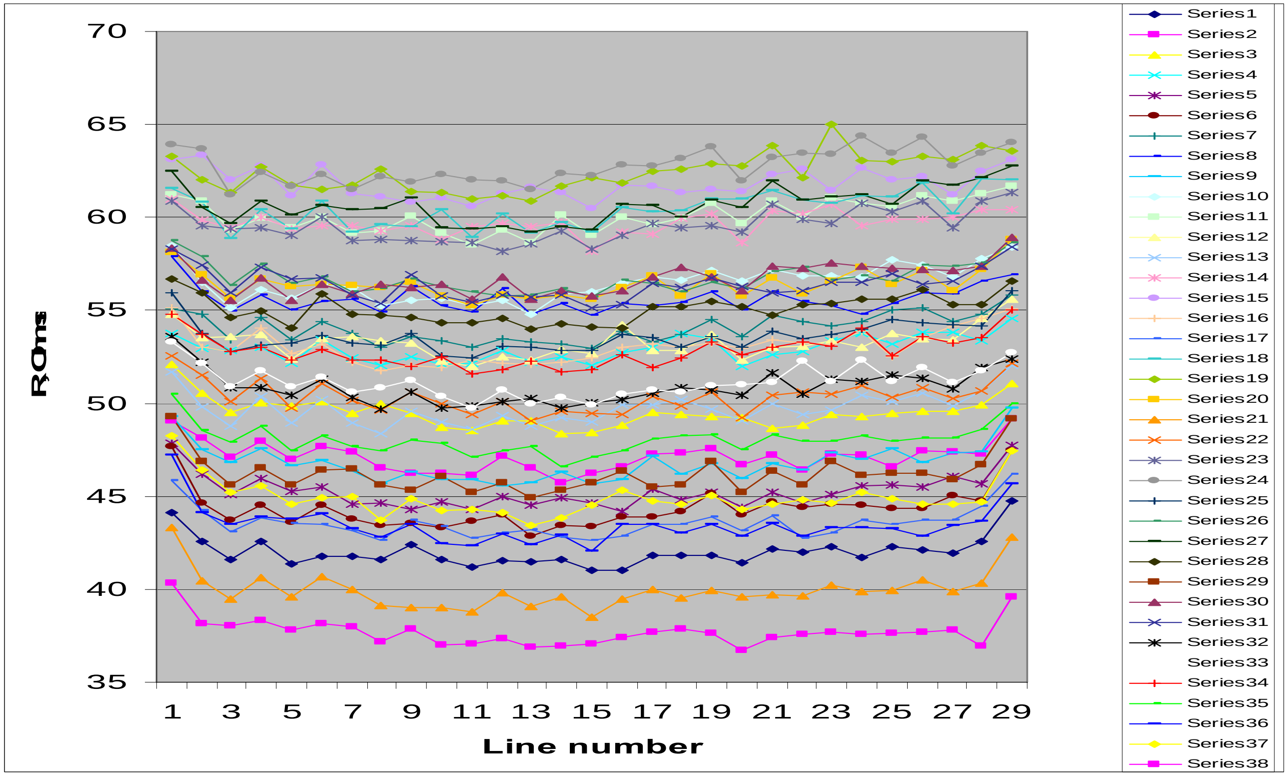


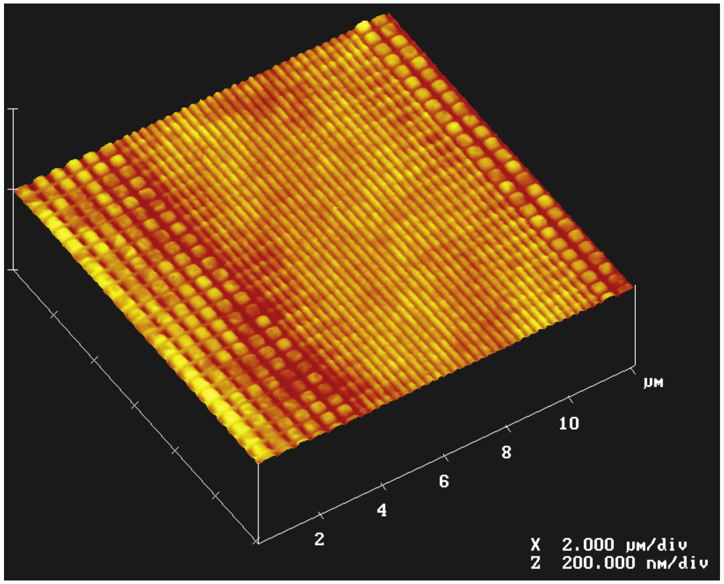
- Connection detail
- DUT Line and global line detail
  - Variable local lines
  - Top/bottom W/S for local and global lines
  - Segmentation of global lines, vertical global lines



Newer modules are much more complex in the number of options and the capability to study more density effects

Test Structures: Real Wire Buss



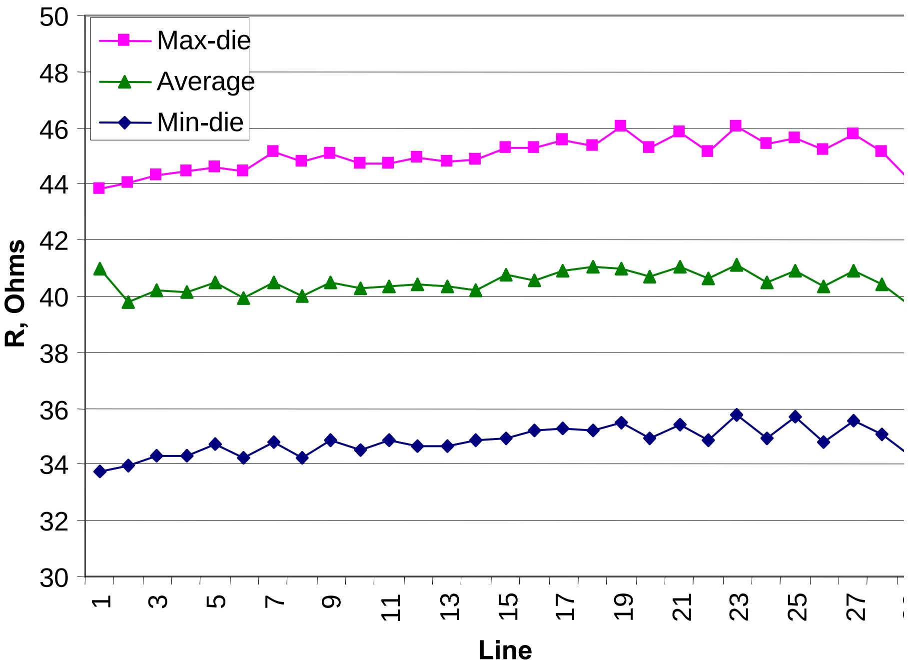


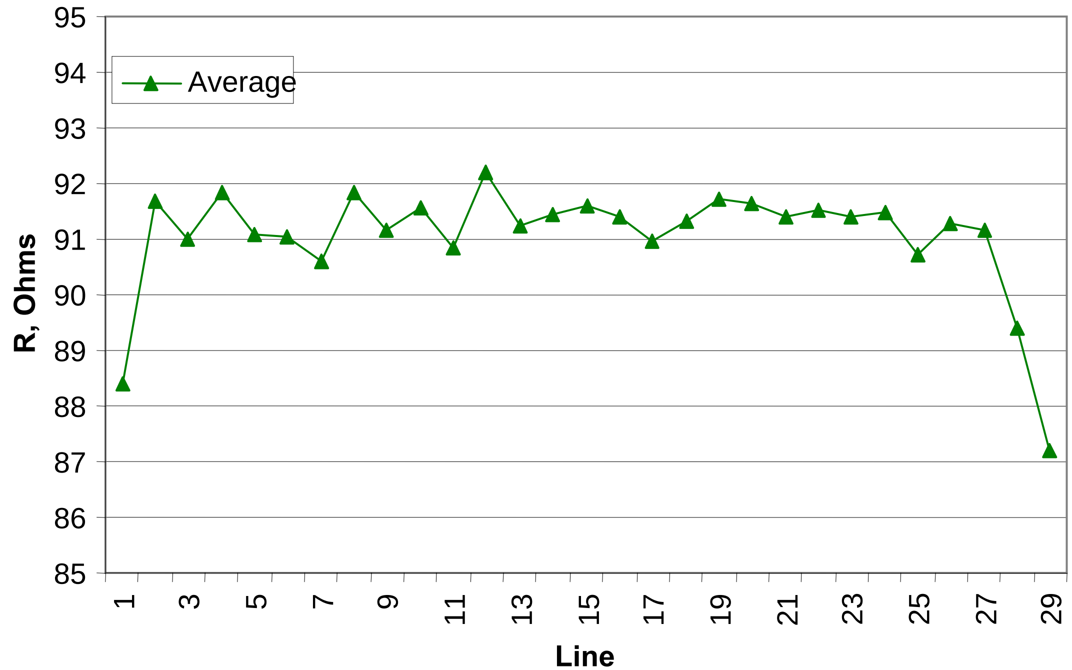
AFM of DUT by Susie Yang.

- 29 lines are in each DUT, the line resistance is measured for each position DUT by DUT
- This shows the variation within one die, and within one wafer

This is a realistic structure representing a real data-buss on a chip. It can help chip designers do better statistical design.

Test Structures: More Real Wire Results





New Process, OPC **Older Process**

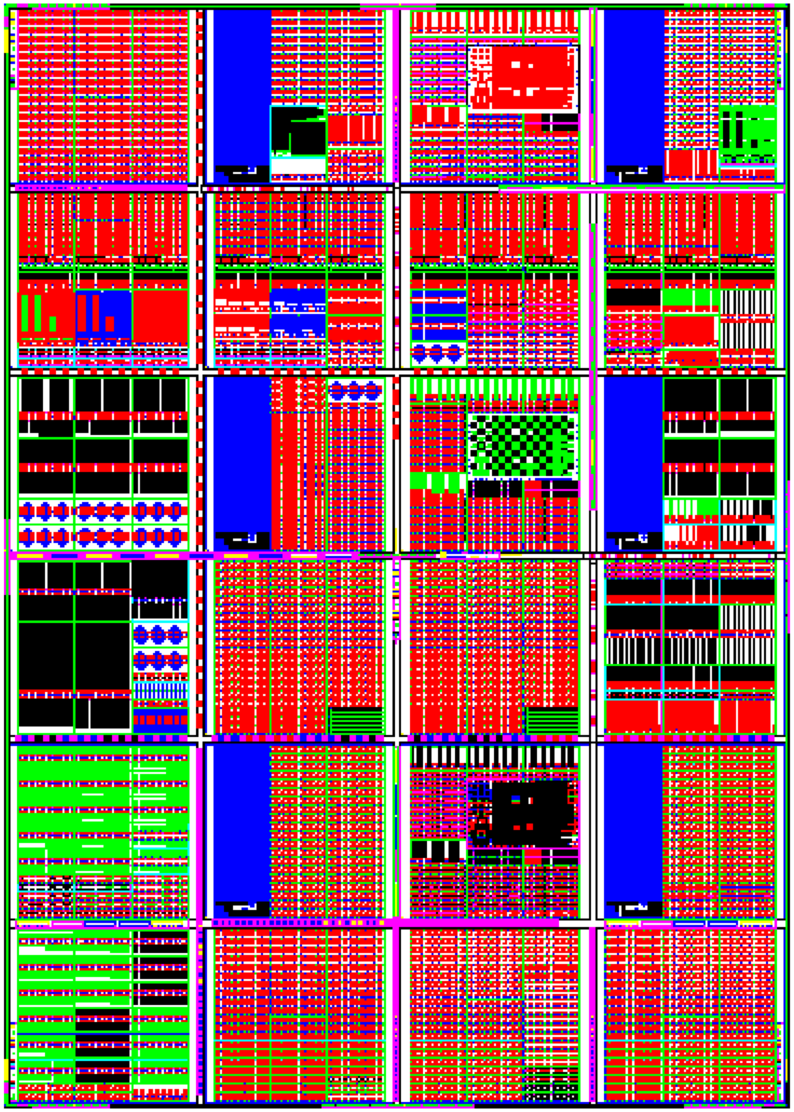
- Within-buss variation is much smaller in the new process and with better OPC.
- Within-wafer variation is smaller in the new processes.

It is very helpful to have the same test structures available to use with different kinds of processes.

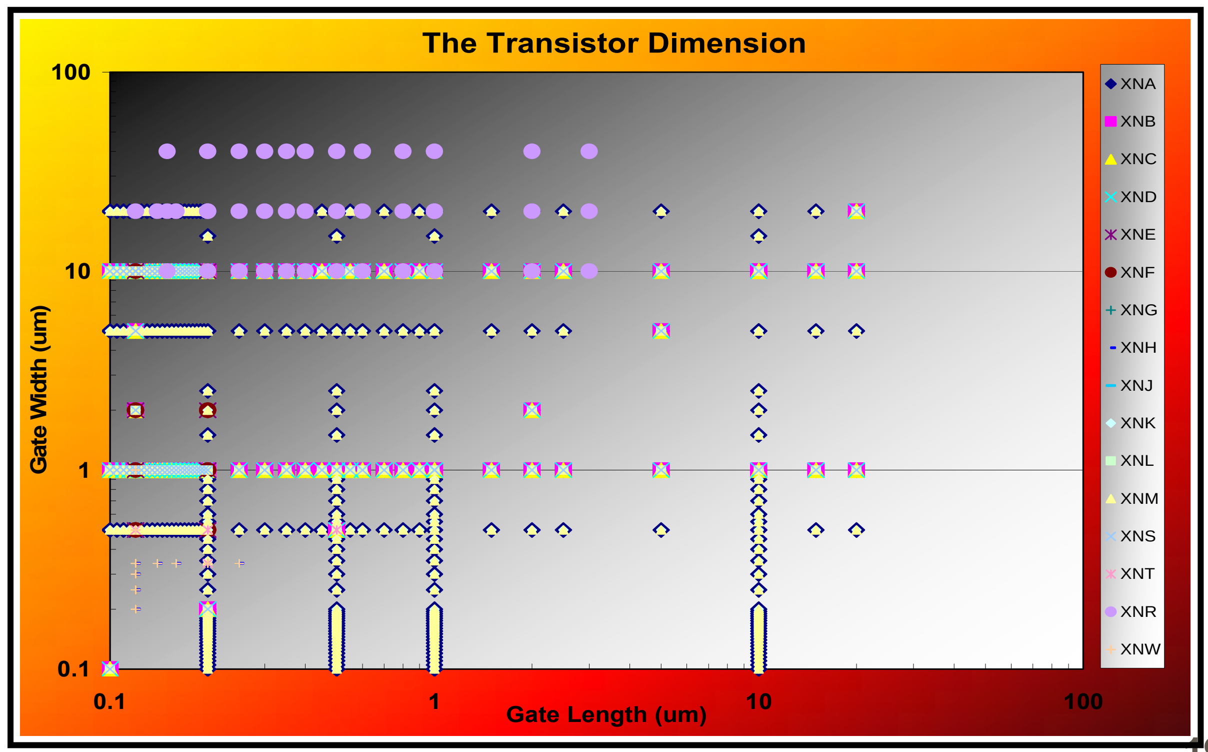
Test Chip Functions

- "Big Enchilada" chips for evaluating design space for devices and interconnect, usually during the technology development phase
  - Large number of DUTs which can be individually probed or accessed through decoding / multiplexing circuits
- Unit process chips focus on a particular piece of equipment and a specific process, like oxide or copper CMP
- Yield chips, which cover a smaller design space and allow separating systematic and random defects
- Production monitoring, often in the scribe lines, with a subset of test structures at the target dimensions

Big Enchilada Test Chip: XD-90

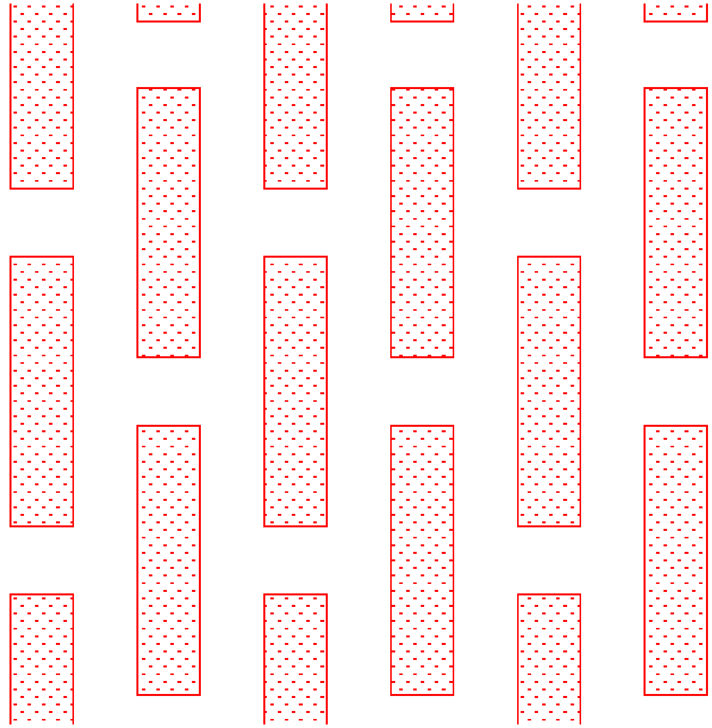


- >900 test modules
- >12500 DUTs
- >3700 Transistors
- Real Wires (>1800 DUTs)
- X Architecture Duts
- Inspection regions
- OCD sites
- Auto-Dummy Fill



Unit Process Test Chip: STI-130

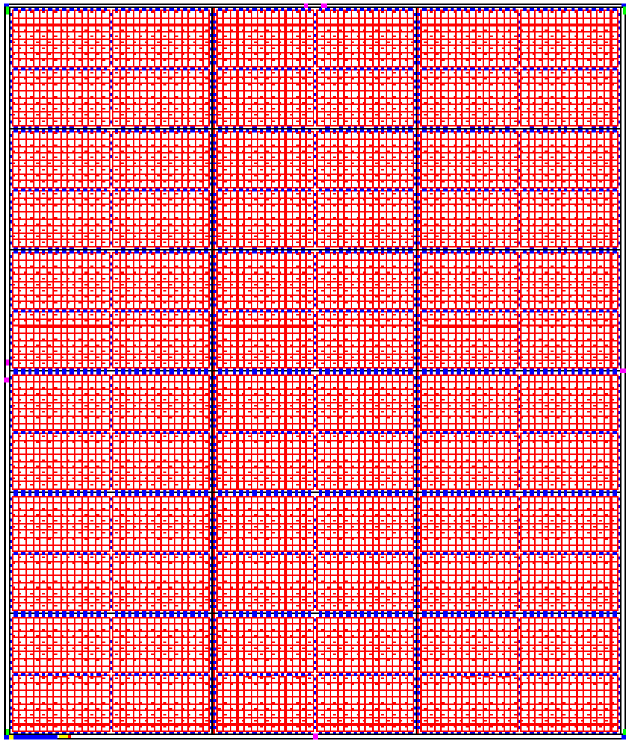
10%	70%	20%	60%	OCD
50%	40%	40%	40%	30%
40%	500um Trench in 40% array	200um Trench in 40% array	100um Trench in 40% array	40%
40%	100um Active in 40% array	200um Active in 40% array	40%	40%
Alt-40%	40%	40%	40%	40%

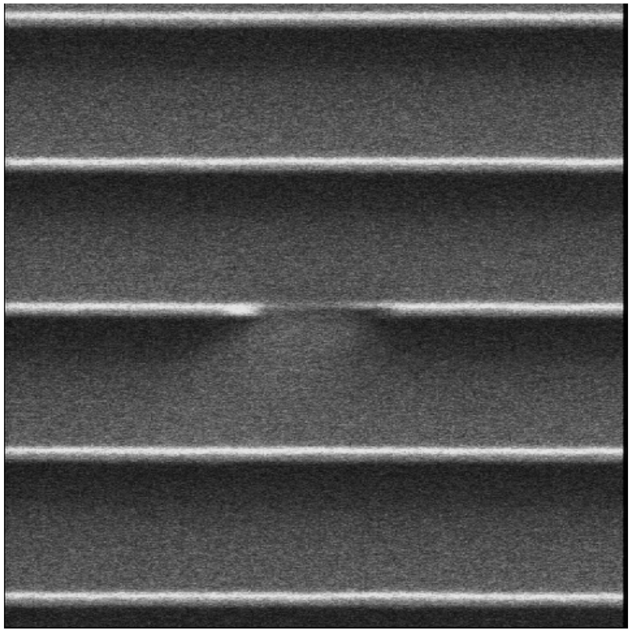


DRAM-like pattern

- 10 – 60% Pattern Density
- Trench and Active Test sites
- OCD sites
- No Dummy Fill – The chips is used for fill rule development!
- No Sub-resolution structures – Do not want yield to limited by litho

Defectivity Test Chip: DM-1





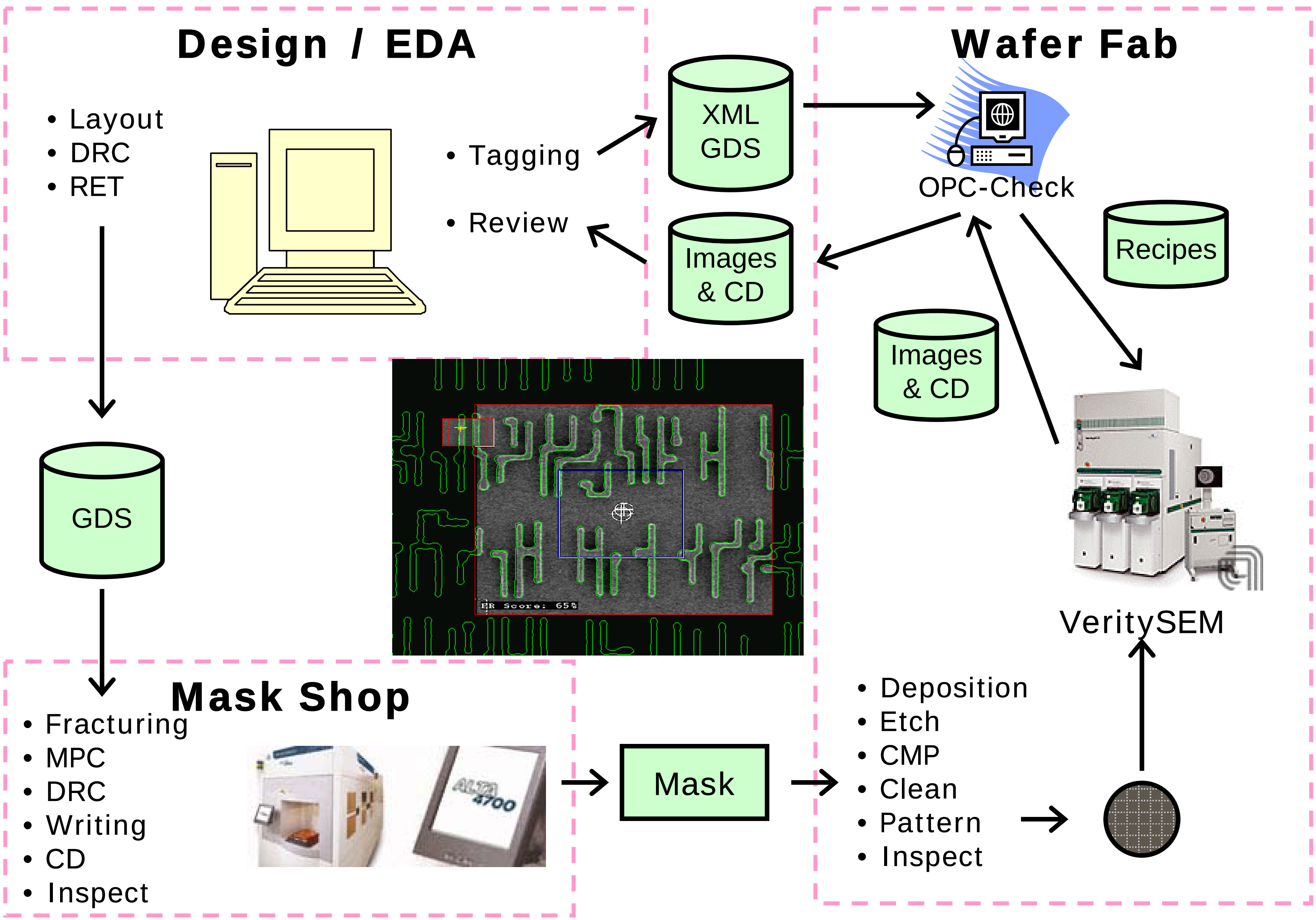
Post-Processing break in a line pattern

- 120 – 250nm features
- Horizontal, vertical lines
- Line Lengths 1 – 200um
- No Dummy Fill
- No Sub-resolution structures

In-Line Structures for Metrology

- Thin Dielectric Film Thickness, n, k
  - Squares large enough to include the measurement beam spot size, typically 50-100um
  - The pattern layers over and under the thin film being measured are important
- Critical Dimensions (CD)
  - Lines, Holes for top-down CD-SEM measurements; use tools like OPC-Check to create recipes for the VeritySEM from layout database tags
  - Lines for Scatterometry (OCD) measurements
  - Lines, Holes for cross-section SEM measurements
- Surface topography
  - Lines for High Resolution Profilometer and AFM measurements
- Doping profile
  - Squares large enough for SIMS measurements, typically 100-200um

In-Line Structures for Metrology: Data Flow



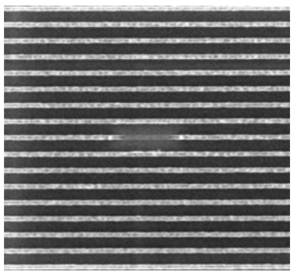
In-Line Structures for Inspection

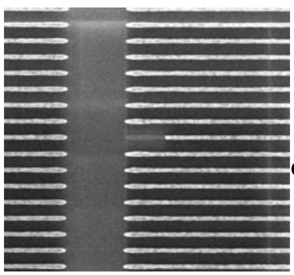
- Systematic Defects
  - Large arrays with different dimensions to determine sensitivity of different structures
  - Analysis tools to “bin” the defects depending on the pattern dimensions
  - Most systematic defects show an increase in the variability of parametric values prior to a hard fail
- Random Defects
  - Range of patterns expected in real chips
  - Arrange structures in the floor plan to simplify recipe creation
  - Include intentional “defects” for calibration and location markers
  - Link data from defect review SEM like SEMVision to the original layout database

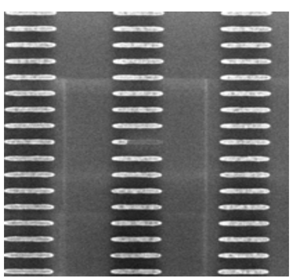
In-Line Structures for Inspection: Binning

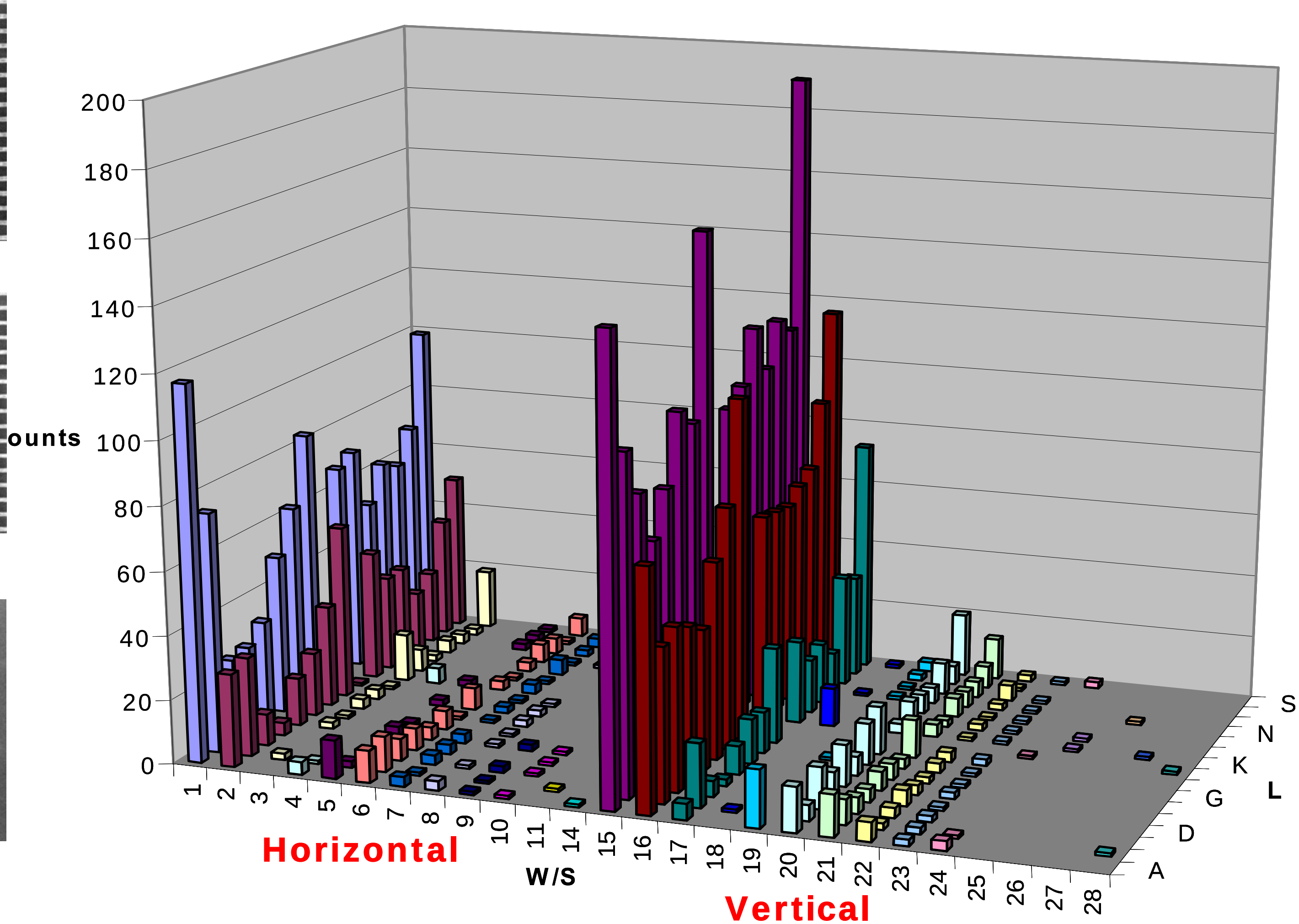
Systematic Defects

- These structures were designed to take defect data from the ComPlus and overlay with the design information to create defect binning by orientation and line-width

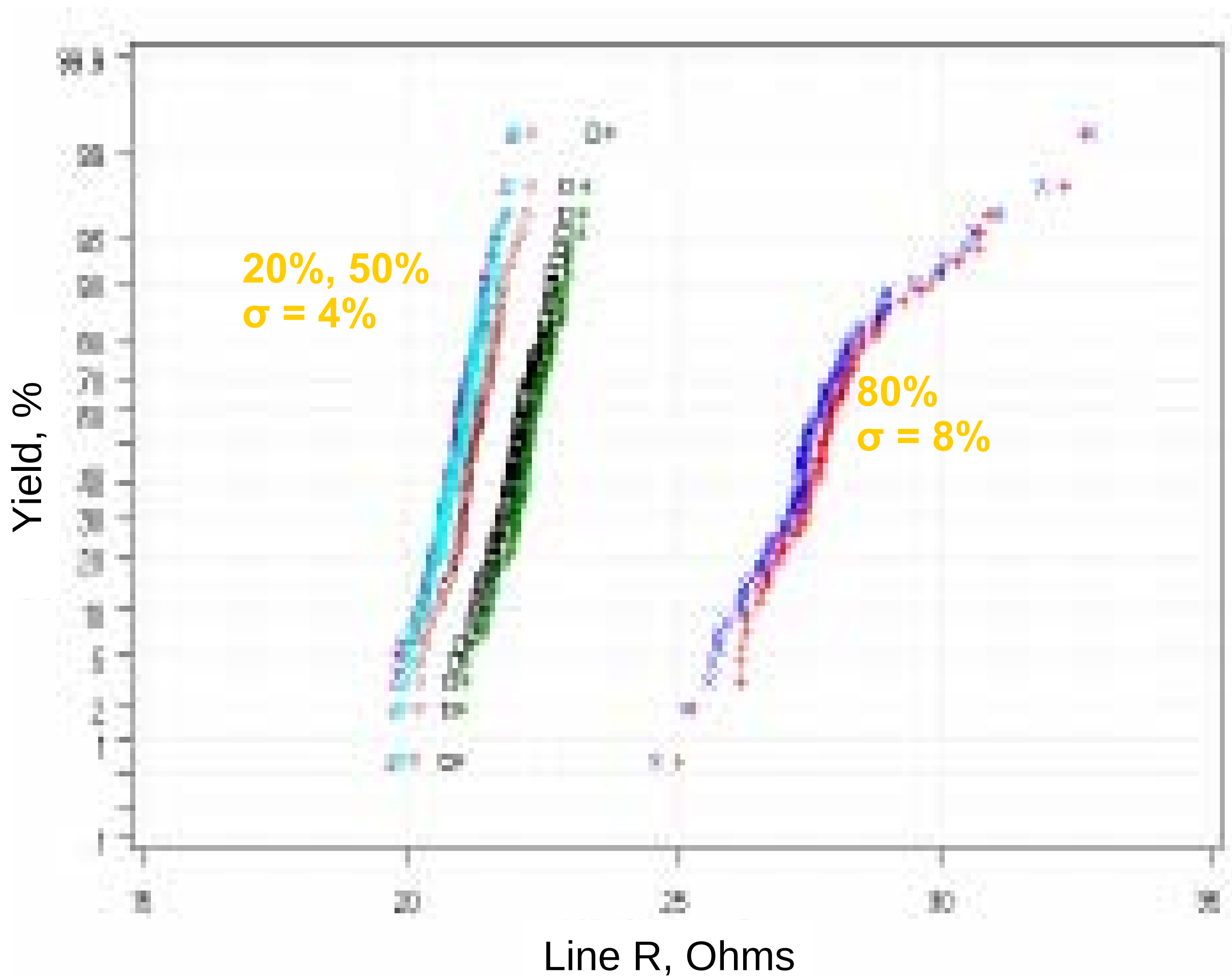






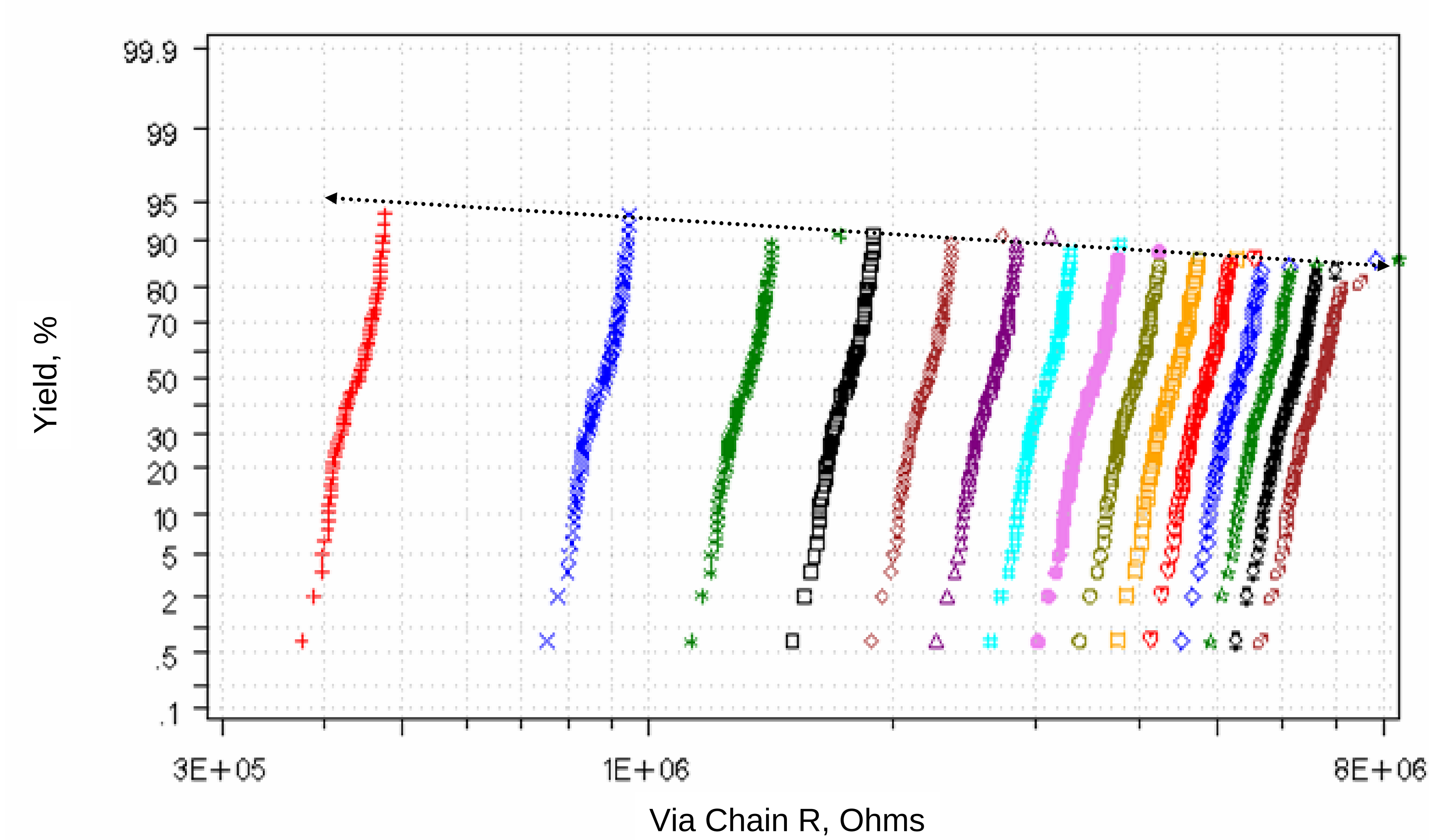


Systematic Defects Structures: Variability



Before the line resistance goes out of spec, the variability has already increased by 2X.

In-Line Structures for Inspection: Random Defects



The yield on long via chains with identical rules shows the random defect density.

Future Design Style Impact on Testchips

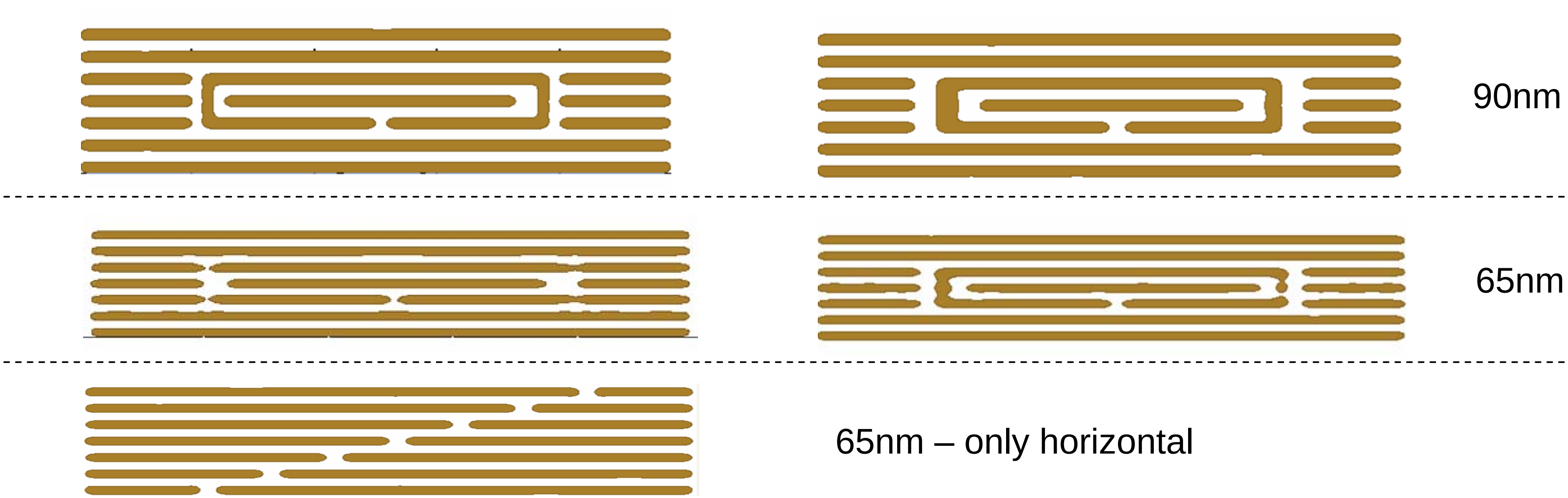
- Today's problem
  - Random Logic layout has many OPC problems, this is going to get worse. The number of RET steps gets longer for each technology generation
  - 2-D layout is the main contributor to the problem; this also causes DUT hook-up problems in testchips
- Future solutions
  - Business-as-usual. Fabs will spend more and more for steppers, designers will spend more and more for RET

    - OR –

  - Designers will adopt much more regular design styles. The layout will mimic gratings, extending the resolution for a given wavelength and numerical aperture. This style will also reduce line-width variability.

Design Style Examples

- **Random logic**
  - The wiring for random logic today uses bends in the M1 to connect transistors. For the 90nm lines shown below, the bent wires print. For 65nm lines, without different rules for spaces and widths, the vertical lines don't appear at all. Even when they appear, the edges are wavy.
  - The "65nm – only horizontal" layout resolves well.
- **Testchips**
  - This implies that a problem is coming for testchip DUT hookup!



Aerial Imaging by Sequoia Cell Designer

Summary

- **Test Structures**
  - Need to separate different pieces of devices into testable elements
  - Details in the structures make a difference
  - Try to make the structures more like real chip layout
- **Test Chips**
  - Separate “big enchilada” designs from unit process and defectivity designs
- **In-Line Structures**
  - Specific structures for metrology are needed; tools are available to link the design database to VeritySEM recipes
  - Inspection can be made more effective with proper design and floor planning
- **Upcoming Issues**
  - 2-D test structures and DUT hook-up will become more difficult to pattern

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  - Valery Alexrad, Andrei Shibkov: Sequoia Design Systems
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References

- Michael C. Smayling, Michael Duane, Raymond Hung, Susie Yang, Shiany Oemardani, “Real Wires: Test Chips Close Gap between Design and Process,” Nanochip Technology Journal, 1-2006, pp 22-29.