







Calibrating Achievable Design
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Outline



- ◆ Motivation: The Design Technology Gap
- ◆ Vision: Open infrastructures that restore design technology productivity (time-to-market, QOR)
- ◆ Strategies and progress on three initiatives
 - ◆ Technology Extrapolation (GTX + Living ITRS)
 - ◆ CAD-IP Reuse (Bookshelf)
 - ◆ Design Process Measurement and Optimization (METRICS)

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Motivation: The Design Technology Gap




- ◆ Design Productivity Gap
 - Threatens quality and value of designs → huge risk to semiconductor industry
- ◆ Design Productivity Gap == Design Technology Productivity Gap
- ◆ Other Themes: change the Design Problem, invent new algorithms, ...
- ◆ This Theme: improve technology development and delivery
- ◆ Mission: improve CAD Industry Productivity by providing open, shared infrastructures that change how we **specify, develop, and measure and improve** Design Technology

Facets of the Design Technology Gap




- ◆ Specification Gap → **What will be the critical design problem?**
 - Need clear industry-wide R&D agenda
 - Need roadmapping of Design Technology vs. ITRS and application markets
- ◆ Development and Delivery Gap → **How to deploy DT better and faster?**
 - Need to reduce Time-to-Market:
 - ◆ 5-7 years to get a leading-edge algorithm into production EDA
 - ◆ → designers battle today's design problems with yesterday's design technology
 - Need to improve QOR:
 - ◆ but, difficult to evaluate impact of new tools on overall design process
 - ◆ published descriptions insufficient for replication or even comparison
 - ◆ → R&D cannot identify, evaluate or reuse the design technology leading edge
 - Need "Foundation CAD-IP": interoperable, reusable, commodity infrastructure
 - ◆ else will over-resource non-strategic, de facto commodity technology
- ◆ Measurement Gap → **Did the envelope of achievable design improve?**
 - Need standard metrics, benchmarks for Design Technology



Vision: Improved Design Technology Productivity

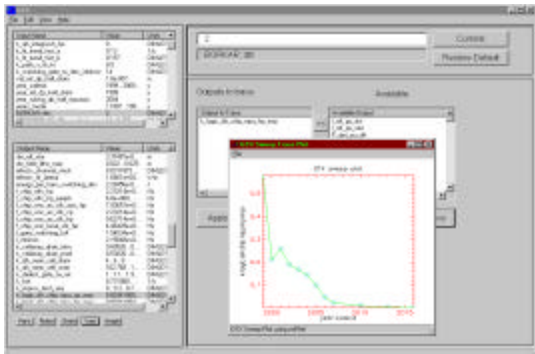
- ◆ Improved design technology planning (“specify”):
 - ◆ What will the design problem look like? What do we need to solve?
 - ◆ Accurate roadmapping for Design Technology
 - ◆ → 1.5x more focused R&D resources
- ◆ Improved execution (“develop”):
 - ◆ How can we quickly (TTM) develop the right design technology (QOR)?
 - ◆ Reusable, commodity, Foundation CAD-IP (+ new publication standards)
 - ◆ → reduce TTM to 2-3 yrs, 2x better leveraged R&D and academic resources, 2x increase in “searched solution space” (mix-and-match flow optimizations)
- ◆ Improved measurement (“measure and improve”):
 - ◆ Did we solve the problem (QOR)? Did the design process improve?
 Did we increase the envelope of achievable design?
 - ◆ Design tool/process metrics, design process instrumentation and CPI
 - ◆ → 1.5x increase in “searched solution space” (flow and process optimizations)

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Strategies 1. Technology Extrapolation

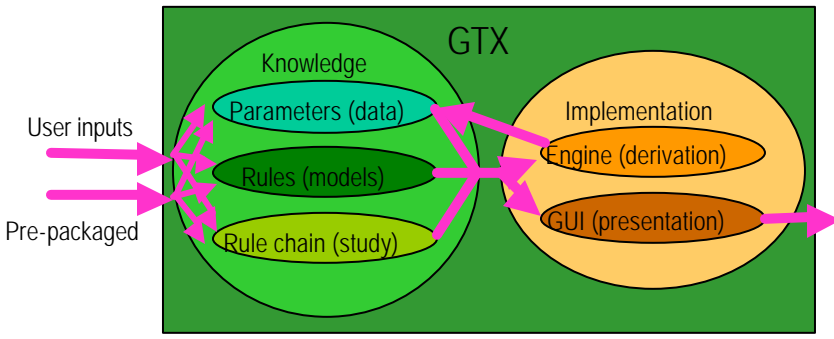
- ◆ Evaluates impact of
 - ◆ design technology
 - ◆ process technology
- ◆ Evaluates impact on
 - ◆ achievable design
 - ◆ design problems
- ◆ What will be the critical design problem?
 - ◆ Variability? Noise? Power? Interconnect? Clocking? Cost?
- ◆ → Roadmapping to drive Design Technology
- ◆ New this year: Calibration of Manufacturing Technology



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GTX: GSRC Technology Extrapolation System

- ◆ GTX = framework for shared technology extrapolation
- ◆ Goals: flexibility, quality, transparency, no redundant effort




- ◆ Open-source: <http://vlsicad.cs.ucla.edu/GSRC/GTX/>
- ◆ Overview: (Oliver poster)

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Progress in Technology Extrapolation


- ◆ “Living ITRS”
 - ◆ First time ever: consistency checks for power, die size, density, performance... among PIDS, A&P, Test, Design, ORTCs, ...
 - ◆ Models and studies to be included along with GTX distribution on ITRS-2001 CD
 - ◆ Integration with other models (e.g., Fisher ITRS-1999 clock frequency)
- ◆ Integrated studies within GTX models:
 - ◆ PIDS: device, device leakage power models
 - ◆ A&P: power, bump/pin counts
 - ◆ Defect Analysis: active area and gate area models
 - ◆ ORTCs: layout density models (SRAM,logic), chip size, max on-chip clock frequency, total chip power
 - ◆ System Drivers: low-power SOC (PDA) model

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Expanded Collection of Models and Studies 

- ◆ “Living ITRS”
- ◆ Design and wafer cost models for logic, DRAM
 - ◆ CMU (Nag, Maly poster)
- ◆ Gate Delay model
 - ◆ UC Berkeley, U. Michigan (Huang, Cao, Sylvester, King, Hu poster)
- ◆ System-in-Package eDRAM / aDRAM cost, resource modeling
 - ◆ UC Santa Cruz (Wang, Dai poster)
- ◆ A Priori Interconnect, Interconnect Performance Predictions
 - ◆ UC Berkeley, U. Michigan, UC San Diego, Ghent (Liu posters)

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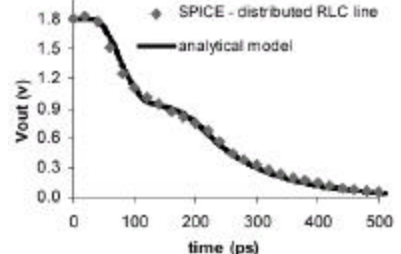
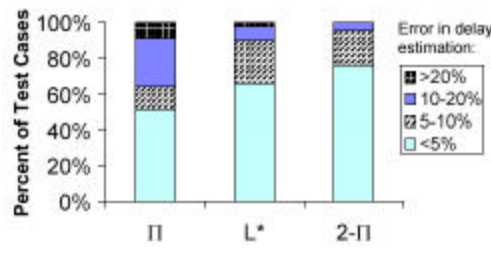
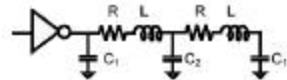
Cost Model - CMU 

- ◆ Design cost model:
 - ◆ W. Maly, “IC Design in High-Cost Nanometer-Technologies Era,” DAC 2001
 - ◆ Models cost per transistor; based on design density index μ tx density
 - ◆ Model parameters extracted from extensive public-domain data (MPU, DRAM)
- ◆ Wafer cost model:
 - ◆ For multi-product / multi-recipe factory; variable # metal layers per product
 - ◆ Tuned to 0.25um CMOS and/or DRAM processes; simple scaling to 0.18um given
 - ◆ Capacity planning tool embedded in the model
 - ◆ Impact of under-utilization of a factory on cost can be estimated
- ◆ URL: http://www.ece.cmu.edu/~pkn/cost_model/
 - ◆ User manual
 - ◆ Excel spreadsheet with 0.25 micron process and cost model.
 - ◆ Excel spreadsheet with design data and design cost model.
 - ◆ A powerpoint tutorial on fabrication process and cost model.

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Gate Delay with RLC Load Model – UCB/Michigan

- ◆ ITRS requires RLC delay model accuracy of 5% @ max chip frequency
 - 25ps accuracy at 130nm node → RC-based load models insufficient
- ◆ Current-source based driver model w/ cut-off, saturation, linear regions
 - Captures non-linear behavior of driver during switching
- ◆ Symmetric 2-P RLC effective loading model
 - Asymmetric models yield mismatch between near- and far-end impedances, and error in wave reflection prediction
- ◆ Analytical driver output waveform expression for increased efficiency

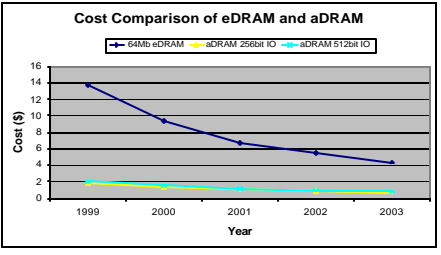
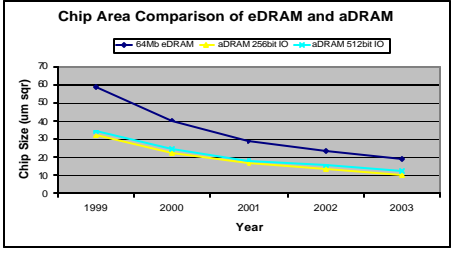


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Area-IO DRAM vs. eDRAM Integration – UCSC

- ◆ System-in-package DRAM-logic integration can be cost-effective alternative to eDRAM
- ◆ Area-IO → tradeoffs of on-chip vs. on-package interconnect, and of application requirements and technology limits vs. memory architecture
- ◆ GTX models: IC, packaging technology; achievable SiP DRAM design



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Expanded Collection of Models and Studies



◆ “Golden” studies → new release, July 2001

- BACPAC, BACPAC_SOI, CriticalPath, Fisher, GateIntDelay, ITRS2001 ORTC
- SUSPENS, Takahashi, device, power, soidevice, soidevice_p, soidevice_n
- Cleanup by U. Michigan
 - ◆ BACPAC model corrections, renaming
 - ◆ Merging of delay and power analyses

◆ 270 GTX Downloads (incl. support files) since last review

- 132 from .edu domains
- 36 from .com, including Compaq, TI, ST Microelectronics, HP, Synopsys, Mentor Graphics, Cypress, Philips, Boeing, Simplex, etc.
- 30 from .net, 8 .jp, 3 .in, 3 .cn

“Living ITRS” and User Support



◆ New feature: “rules calling rules as functions”

◆ New Excel-GTX utilities

- Many models originally captured in MS Excel files → new utilities aid making and checking corresponding GTX studies
- Rule-making utility from Excel file, dictionary file
- Rule-fitting utility for “hardcoded” rows
- Comparison utility takes GTX, Excel files and compares study results

◆ Near-term plans – user support

- Multiple rule chains, back-solving, namespace handling, calculator *if*, cleanups

◆ Near-term plans – models and studies

- Memory/FIFO models (Cypress, UCSC, UCSD), inductance / SOI / device models (Michigan), variability (IBM, Michigan, UCSD), ...
- Cost, revenue models to support research on design for manufacturing variability
- Additional ITRS-2001 models: eDRAM adoption, low-power SOC driver, high-speed signaling, package/die cost and bump/IO count, ...

Strategies 2. CAD-IP Reuse



- ◆ **Rapid development and evaluation via CAD-IP reuse**
- ◆ **CAD-IP = Data models and benchmarks**
 - ◆ context descriptions and use models
 - ◆ testcases and good solutions
- ◆ **CAD-IP = Algorithms and algorithm analyses**
 - ◆ mathematical formulations
 - ◆ comparison and evaluation methodologies for algorithms
 - ◆ executables and source code of implementations
 - ◆ leading-edge performance results
- ◆ **CAD-IP = Traditional (paper-based) publications**

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The GSRC Bookshelf: A Repository for CAD-IP



- ◆ **New element of VLSI CAD culture**
 - ◆ *“Community memory”*
 - ◆ data models, algorithms, implementations
 - ◆ Repository for open-source Foundation CAD-IP
 - ◆ *Publication medium* that supports efficient CAD R&D
 - ◆ benchmarks, performance results
 - ◆ algorithm descriptions and analyses
 - ◆ quality implementations (e.g., open-source UCLA PDTools)
- ◆ **Enables comparisons to identify best approaches**
- ◆ **Enables communication by industry of use models, problem formulations**
- ◆ **<http://gigascale.org/bookshelf>** , IEEE Design & Test paper to appear
- ◆ **Overview: (Markov poster)**

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Progress in CAD-IP Reuse



- ◆ On-going GSRC Bookshelf expansion → 27 slots and 90+ entries
 - NEW this year (not including "picked off the Web"):
 - Incremental SAT: **SATIRE**
 - Variable ordering for SAT, BDD: **MINCE**
 - Floorplanners (Java source) (**Wu, Dai poster**) (C++ source) (**Adya/Markov poster**)
 - Placers: **Feng Shui** (C source), Dragon (planned source)
 - Global router: **Labyrinth** (C++ source)
 - RLC delay calculator: **HIDE** (C source)
 - Global routing formats (planned C++ source)
 - Cadence's open-source **LEF/DEF parsers in UCLA DB**
 - **PERL/Tcl/Python interfaces** for UCLA DB
 - **Scan-chain** (C++ source)
 - **RSMT/RMST, Buffered ST** (C++ source) (**Liu, Mandoiu posters**)
 - **Single Interconnect-Tree Synthesis** (C++ source)
- ◆ Users in industry
 - Vertical benchmark designs
 - IBM Austin: bookshelf placers integrated with IBM ChipBench
 - Intel Santa Clara : converters to/from Bookshelf formats; expts with Bookshelf source
 - Many EDA companies
- ◆ Users in academia
 - Y. Deng and W. Maly (CMU) , ISPD 2001 (placer *source code reuse*)
 - X. Yang, E. Bozorgzadeh and M. Sarrafzadeh (UCLA), SLIP 2001, used 3 placers
 - P. Madden (SUNY), DAC 2001, used two placers + benchmarks

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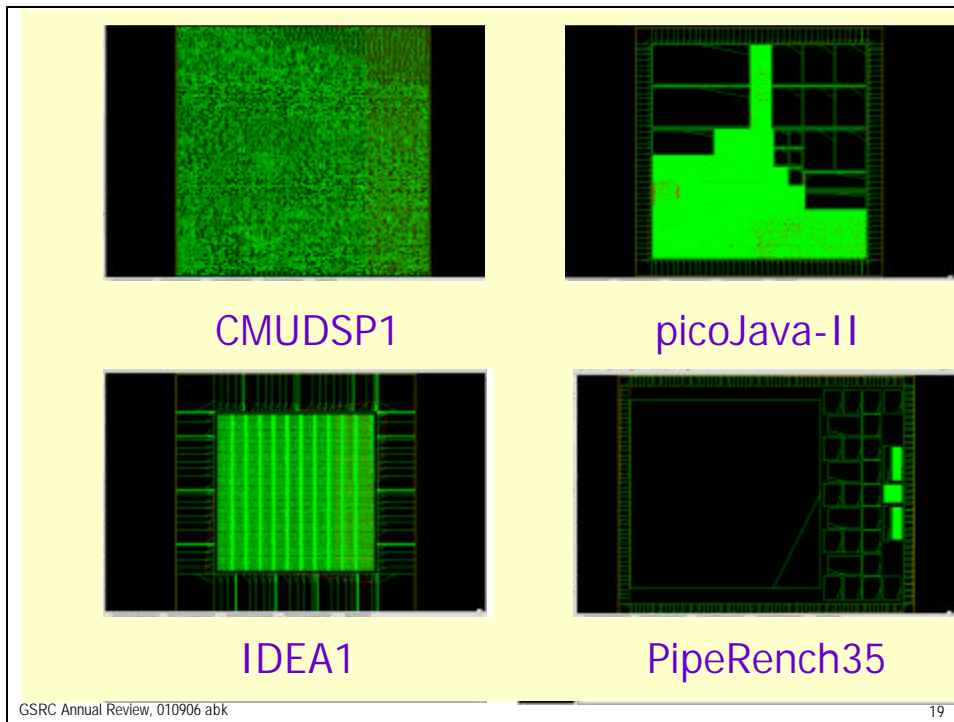
Vertical Benchmark Designs - CMU



Benchmark	Components	Style	Clock	Route	Testbench
picoJava-II	119,871	Blocks & Cells			
CMUDSP1	18,863	Cells			
PipeRench18	99,208	Blocks & Cells			
PipeRench35	9797	Blocks & Cells			
IDEA1	37,657	Cells			
IDEA2	8,450	Cells			

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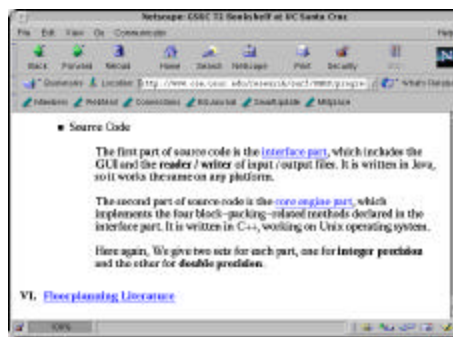
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Java Floorplanner - UCSC



◆ New in the slot:



Source code of the floorplanner
 (Interface + Core Engine) is
 available in the slot



◆ (New issue: delivering support for slot users)

Near-Term Foci



- ◆ Vertical Benchmarks (CMU)
- ◆ Integrated (RTL-to-layout) implementation flows
 - Data model consolidation, adjustments within Bookshelf for industry SP&R integration
 - ◆ E.g., working Cadence SE-PKS (CapoT → Pearl → WarpRoute → Pearl)
 - ◆ E.g., planned IBM ChipBench (CapoT → EinsTimer → Xrouter → EinsTimer)
 - OpenAccess compatibility (currently assumed via compatibility with LEF/DEF)
 - Goal: full open-source flows
- ◆ Evaluation infrastructure – e.g., algorithm server
- ◆ Separations (e.g., g-d route), unifications (e.g., FP-place), objectives
- ◆ Adoption metrics (goal: “double each year”)
 - Publications at ACM/IEEE conferences and workshops (Fall '00 – Summer '01)
 - ◆ Enabled by the Bookshelf (3); codes submitted to the Bookshelf (3 more)
 - ◆ Starting to track coverage, quality, status (conferences, problem lists)
 - tar.gz downloads of Bookshelf material
 - ◆ UCLA web logs (Sep 1, 2000 – Aug 24, 2000): 295
 - ♦ 126 .edu, 38.com, 42 .net, 15 .de, 11 .in, 9 .fr, 6 .jp, 5 .uk
 - ◆ openeda.org (June 1, 2000 – Aug 24, 2000): 315

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VLSI CAD/Design Education and the Bookshelf



- ◆ Bookshelf can boost VLSI design and design technology education
 - Industry-relevant, open-source design tools, methodologies, design projects
 - Systematic development of interoperability, supporting materials, community
- ◆ Used in layout classes, undergraduate research projects at U. Michigan
 - Example: Connect Cadence's LEF/DEF parsers to UCLA DB
 - ◆ Now available in Bookshelf under *UCLA PD tools*
 - Example: Devise global routing formats (<http://vlsicad.eecs.umich.edu/BK/route/>)
 - ◆ Satisfy **typical use models** (e.g., LEF/DEF-based flows)
 - ◆ Identify insufficiencies in existing global-route formats
 - ◆ Provide detailed **Web-based documentation, examples**
 - ◆ Create **parsers and basic data structures in C++**
 - ◆ **Connect to existing global router** (*Labyrinth* from UCLA)
- ◆ Bookshelf tools easier to learn and understand
 - Simpler, transparent formats, code, formulations,... yet industry-interoperable
 - More meaty courses possible (e.g., with vertical benchmarks)
 - → New graduates more knowledgeable, more valuable

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Strategies 3. METRICS

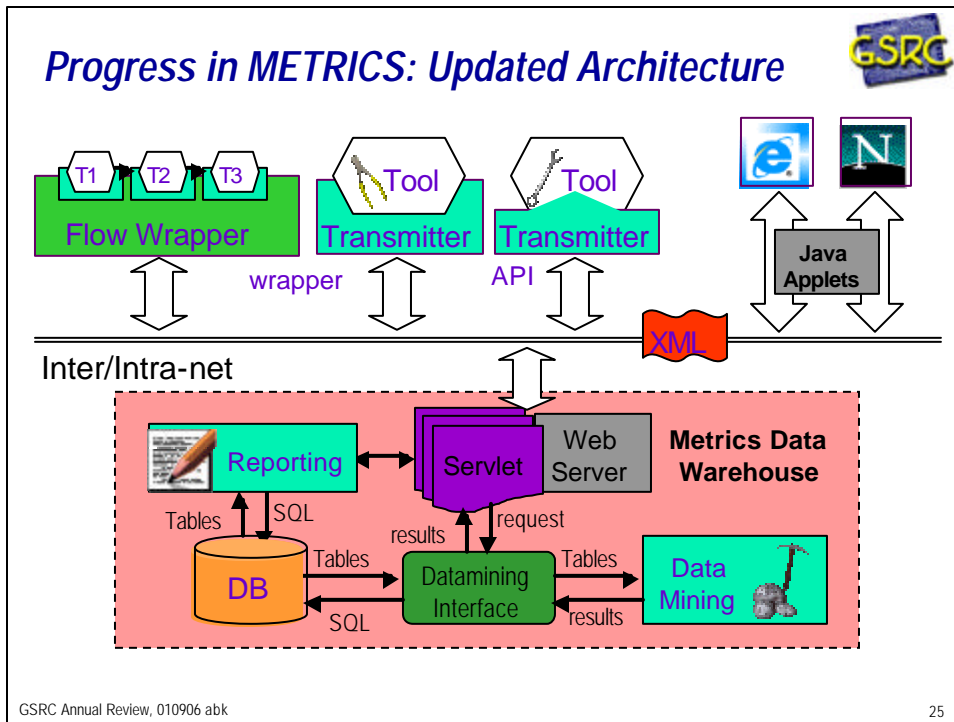


- ◆ **Did I really solve the problem?**
- ◆ **Requires understanding of:**
 - ◆ what should be optimized by which heuristic
 - ◆ design as a process
- ◆ **METRICS = standard infrastructure for measuring and optimizing the semiconductor design process**
- ◆ **“Measure, then improve”**
 - ◆ design becomes more of a formal discipline
- ◆ **Infrastructure**
 - ◆ design process data collection
 - ◆ data mining, visualization, diagnosis

Benefits of METRICS



- ◆ **Benefits for design project management**
 - ◆ accurate resource prediction at any point in design cycle
 - ◆ accurate project post-mortems
- ◆ **Benefits for Design Technology R&D**
 - ◆ identification of tool sweet spots, key instance parameters
 - ◆ identification of design-process-relevant optimization objectives
 - ◆ feedback from design activity regarding tool, parameter usage
 - ◆ “no more log files”
- ◆ **Open-source system: <http://vlsicad.cs.ucla.edu/GSRC/METRICS>**
- ◆ **Overview: (Mantik poster)**



- ### Progress in METRICS
-
- ◆ METRICS integration with flow manager, recording of flow metrics
 - E.g., used to characterize benefits of wireload models in timing-driven design
 - ◆ METRICS integration with data mining and statistics tools (e.g., "R")
 - Enables estimation of best configuration of tool parameters for given instance
 - ◆ Design metrics (design quality normalization) survey
 - <http://vlsicad.cs.ucla.edu/GSRC/METRICS>
 - ◆ Opportunistic uses of METRICS
 - By tracking timing information, METRICS allowed identification of a "temporal Rent" timing-structural characterization of timing-driven designs
 - ◆ Near-term goals
 - Close METRICS-tools loop, so that tools can use METRICS to obtain best parameter settings for a given design and runtime/quality requirement
 - Explore ability to characterize tools' sweet spot
 - Improved UI for the METRICS system's data mining and statistics capabilities
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Integration with Datamining and Statistics Tools

- ☆ Design instances and design parameters
 - attributes and metrics of the design instances
- 🕒 CAD tools and invocation options
 - list of tools and user options that are available
- 🕒 Design solutions and result qualities
 - qualities of the solutions obtained from given tools and design instances
- ◆ Given ☆ and 🕒, estimate the expected quality of 🕒
 - e.g., runtime predictions, wirelength estimations, etc.
- ◆ Given ☆ and 🕒, find the appropriate setting of 🕒
 - e.g., best value for a specific option, etc.
- ◆ Given 🕒 and 🕒, identify the subspace of ☆ that is “doable” for the tool
 - e.g., category of designs that are suitable for the given tools (“sweet spot”)

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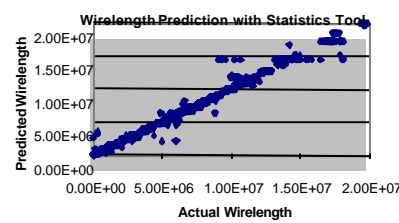
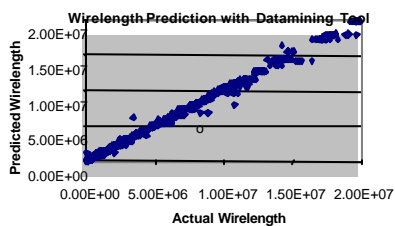
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Examples

- ◆ Sample classification rule (from “R” statistics package):

if (NumRoutingLayer ∈ 3, CoreWidth ∈ 1092, CongMode2 = false, TimingMode = false) then
Wirelength = 7.0756e+06 - 167 NumCells - 997114 NumLayer; else

if (NumRoutingLayer ∈ 3, CoreWidth ∈ 1092, CongMode2 = true, TimingMode = false) then
Wirelength = -1.30109e+06 + 4994 CoreWidth - 4452 CoreHeight + 11710 CongMaxUtil - 1
NumCells + 228663 CutRatio - 16898 NumLayer; else ...



- ◆ Parameters and best values for low-congestion solutions

Parameter Name	Description	Value Range
annealingRefinement	Use annealing refinement	true
congMaxUtil	Max utilization	67.1364 - 83.1284
congMode2	Use new congestion model	true
congPenaltyThreshold.h	Horizontal threshold penalty	0.2571 - 0.5378
congPenaltyThreshold.v	Vertical threshold penalty	0.1126 - 0.5476
placeIONetWeight	Weight for placed IO net	0.5376 - 0.9812
cutRatio	Cut ratio	0.4010 - 0.7307

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Ref: A. B. Kahng and S. Mantik "A System for Automatic Recording and Prediction of Design Quality Metrics", ISQED-2001 Best Paper

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Summary: Improved Design Technology Productivity

- ◆ **Promote cooperative cultures and open infrastructures that enable better creation of design technology**
- ◆ **Improved vision and design technology planning (“specify”):**
 - What will the design problem look like? What do we need to solve?
 - **Answer: Calibration of Manufacturing Technology, and Technology Extrapolation (GTX)**
- ◆ **Improved execution (“develop”):**
 - How can we quickly develop the right design technology (TTM)?
 - **Answer: CAD-IP Reuse (Bookshelf)**
- ◆ **Improved measurement (“measure and improve”):**
 - Did we solve the problem (QOR)? Did the design process improve?
Did we increase the envelope of achievable design?
 - **Answer: Design Process Instrumentation, Optimization (METRICS)**