C.A.D. Initiatives

◆ Specification Gap: e.g., What will be the critical design problem?
  ♦ GTX
  ♦ GTX models include canned optimizations = canned design space explorations

◆ Development and Delivery Gap: e.g., How to deploy DT better/faster?
  ♦ Bookshelf

◆ Measurement Gap: e.g., Did achievable design improve?
  ♦ Metrics
  ♦ Definition of success

◆ (Next up: Education? Measuring research process?)

◆ Shared Context Is A Force Multiplier
Living Roadmap

- Network, telecommunications, embedded computing systems
  - Synchronous buses → 1Gbps, differential signaling → 10Gbps
  - Network, optical interfaces have multipliers of 10x, 4x (faster than device density, speed)
  - Train wrecks: chip-to-package and system-level interconnects (materials, signaling standards, implementation costs), power, design TAT, cost

- Appropriate metrics are “non-traditional”: density, cost, performance, power, and RAS (reliability, availability, and serviceability)
  - Density: connections and bandwidth per cm$^{2,3}$, watts/m$^3$
  - Performance: How many interconnect/cm$^{2,3}$? How long are traces? What types of signals, and what voltage levels, will meet signaling rate needs?
  - Cost: decompositions (mother, switch/routing, control, port interface, application), and dimensions (per (gE, FC, DWDM, ...) port, Gbps, MIPS, $...$)
  - RAS: unintentionally / intentionally (for func) dropped bits/packets dropped, failure rates

- Many models to build and integrate: SOC integration (what is integratable, at what cost), analog circuits/DT (how badly do these fail to scale), design quality and cost, power (circuits, multi-Vdd/Vt/tox / biasing, GALS/GSLA, ...), manufacturing interface (variability, NRE, layout densities, ...)

- GTX within DT: What are the key design technology needs?
  - Application roadmap (= ITRS System Drivers Chapter = complement to ITRS ORTCs)
  - Application product ROI = value/cost (= attributes not yet well-defined/-measured)
  - Impacts of Design Technology (== Metrics initiative)
Goal is to produce component-based, application-specific design methodologies and flows

- How will the methodology space be explored, and flows prototyped?
- Where are the reusable components?

Open-source (understandable, reusable), malleable DT components

- Centered on back end, completely missing AMS capabilities, ...

Common data model and access mechanism (and repository?)

- OpenAccess source code release

Design Drivers very close to vertical benchmarks (= existing Bookshelf slot)

- Recent overtures from IBM, LSI w.r.t. OpenAccess, working vertical benchmarks
- Potential work with Fabrics on snap-on flows, etc.

KEY: Common DT Infrastructure

Other: synergy with education in VLSI design, design technology
**Metrics**

- **Goal:** measure and improve
  - Systems
  - Processes

- **Relevant system attributes / metrics**

- **System value**

- **System cost (design, production)**
  - From system ROI, have a platform from which to evaluate technology ROI

- **Technology cost (research, advanced research, development, ...)**

- **Supporting technologies / infrastructures (data mining, parameter identification, model fitting)**

- **Other: Research process**
  - What is the impact of FCRP? (# newspaper articles? # papers? Coauthorship statistics? Survey results? Scientific health of (Design/Test, Interconnect, etc.) communities?) == part of original “Measure and Improve” goals
“Living ITRS-2001” in GTX

- First time ever: consistency checks, unified assumptions for power, frequency, die size, density, performance
- Creates linkages between Design, Assembly/Packaging, Defect Reduction, Process Integration / Devices / Structures, Test, Overall Roadmap Technology Characteristics, ...
- Models and studies are linked with ITRS-2001 distribution
- Improves flexibility, quality, transparency of roadmapping
  - Allows semiconductor industry to better allocate R&D investment: “Who should solve a given red brick wall?”
- 2002 goal: Increase fraction of ITRS captured within GTX