Calibrating Achievable Design

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Motivation: The Design Technology Gap

Vision: Create open, shared infrastructures that restore design technology productivity (time-to-market, QOR)

Strategies: Three Initiatives, plus culture change

- Technology Extrapolation (GTX + Living ITRS)
- CAD-IP Reuse (Bookshelf)
- Design Process Measurement and Optimization (METRICS)

Progress against Strategies
Motivation: The Design Technology Gap

- Design Productivity Gap
  - Well-documented, threatens quality and value of designs
  - $\rightarrow$ huge cost to semiconductor industry

- Other themes: change the Design Problem, invent new algorithms, ...

- Design Productivity Gap $==$ Design Technology Productivity Gap

- Problem: Improve Time-To-Market and Quality-of-Result for Design Technology

- This Theme: improve CAD Industry Productivity by changing how we specify, develop, and measure and improve Design Technology
Facets of the Design Technology Gap

Facets

- No clear industry-wide R&D agenda
- Time-to-Market: 5-7 years to get a leading-edge algorithm into production EDA
  - designers battle today’s design problems with yesterday’s design technology
- QOR: difficult to evaluate impact of new tools on overall design process
- QOR: published descriptions insufficient for replication or even comparison of algorithms
  - CAD R&D cannot identify, evaluate or reuse the CAD technology leading edge
  - research and innovation stall

Causes

- Lack of clear roadmapping for Design Technology w.r.t. ITRS, application markets
- Lack of “Foundation CAD-IP”: interoperable, reusable, commodity infrastructure
- Lack of resources, and relative over-resourcing of non-strategic, de facto commodity technology
- Lack of standard metrics, benchmarks for Design Technology
- More maturity needed w.r.t. control, strategic-vs-commodity distinction, etc.
Vision: Improved Design Technology Productivity

- This Theme promotes mature, coopetitive cultures and shared, open infrastructures that lead to improved creation of design technology.

- Improved vision and design technology planning ("specify"):
  ▲ What will the design problem look like? What do we need to solve?

- Improved execution ("develop"):
  ▲ How can we quickly develop the right design technology (TTM)?

- Improved measurement ("measure and improve"):
  ▲ Did we solve the problem (QOR)? Did the design process improve? Did we increase the envelope of achievable design?
“A Vision of the Future”

- **Improved vision and design technology planning (“specify”):**
  - ▼ What will the design problem look like? What do we need to solve?
  - ▲ Accurate roadmapping for Design Technology
  - ▼ → 1.5x more focused R&D resources

- **Improved execution (“develop”):**
  - ▼ How can we quickly develop the right design technology (TTM)?
  - ▲ Reusable, commodity, Foundation CAD-IP (+ academic publication standards)
  - ▼ → reduce TTM to 2-3 yrs, 2x better leveraged R&D and academic resources, 2x increase in “searched solution space” (mix-and-match flow optimizations)

- **Improved measurement (“measure and improve”):**
  - ▼ Did we solve the problem (QOR)? Did the design process improve? Did we increase the envelope of achievable design?
  - ▲ Design tool/process metrics, design process instrumentation and CPI
  - ▼ → 1.5x increase in “searched solution space” (flow and process optimizations)

- **Design Technology Productivity improves Design Productivity**
Strategies 1. Technology Extrapolation

◆ Evaluates impact of
  ▲ design technology
  ▲ process technology

◆ Evaluates impact on
  ▲ achievable design
  ▲ associated design problems

◆ What do we need to solve?

◆ What will the design problem look like?

◆ == Roadmapping to drive Design Technology

◆ Years 3 onward: Calibration of Manufacturing Technology

What is the most power-efficient noise management strategy?

How and when do L, SOI, SER, etc. matter?

Will layout tools need to perform process simulation to effectively model cross-die and cross-wafer manufacturing variation?
Optimal Repeater Sizing

- Most commonly used optimal repeater sizing expression (Bakoglu)

\[ S = \sqrt{\frac{R_D C_{\text{int}}}{R_{\text{int}} C_{\text{in}}}} \]

- New study:
  - \( \Delta \) Sweep repeater size for single stage in the chain
  - \( \Delta \) Examine both delay and energy-delay product

![](image)
**Cu Resistivity: Effect of Line Width Scaling**

**Effect of 5 nm Barrier**
- Conformal 5 nm barrier assumed
- Even a 5 nm barrier will increase resistivity drastically

**Effect of Electron Scattering**
- No barrier assumed
- Electron scattering increases resistivity
- Lowering temperature has a big effect

**Source:** MARCO IFRC
Goal: **Shared Technology Extrapolation System**

- **Flexibility**
  - edit or define new parameters and relations between them
  - perform specific studies (but different studies at different times)

- **Quality**
  - continuous improvements
  - world-wide participation of experts

- **Transparency**
  - open-source mechanism
  - models visible to the user

- **No more redundant effort**
  - permanent repository of first choice
  - adoptability and maintainability
GTX: GSRC Technology Extrapolation System

- GTX = framework for shared technology extrapolation

Open-source: http://vlsicad.cs.ucla.edu/GSRC/GTX/
Strategies 2. CAD-IP Reuse

How can we quickly develop the right design technology?

Analogy: Hardware Design :: CAD Tool Design

- Hardware design is difficult
  - complex electrical engineering and optimization problems
  - mistakes are costly
  - verification and test not trivial
  - few can afford to truly exploit the limits of technology
  - A Winning Approach: Hardware IP reuse

- CAD tools design is difficult
  - complex software engineering and optimization problems
  - mistakes can be showstoppers
  - verification and test not trivial
  - few can manage complexity of leading-edge approaches
  - A "Surprising Proposal": CAD-IP reuse
What is CAD-IP?

- Data models and benchmarks
  - context descriptions and use models
  - testcases and good solutions

- Algorithms and algorithm analyses
  - mathematical formulations
  - comparison and evaluation methodologies for algorithms
  - executables and source code of implementations
  - leading-edge performance results

- Traditional (paper-based) publications
The GSRC Bookshelf: A Repository for CAD-IP

Culture change

- "Community memory” for CAD-IP
  - data models, algorithms, implementations

- Publication medium that enables efficient CAD R&D
  - benchmarks, performance results
  - algorithm descriptions and analyses
  - quality implementations (e.g., open-source UCLA PDTools)

Simplified comparisons to identify best approaches

Easier for industry to communicate new use models

Eventually: repository for open-source Foundation CAD-IP

http://vlsicad.cs.ucla.edu/GSRC/bookshelf
Strategies 3. METRICS

◆ Did I really solve the problem?
◆ Requires understanding of:
  ▲ what should be optimized by which heuristic
  ▲ design as a process
◆ METRICS = standard infrastructure for measuring and optimizing the semiconductor design process

◆ “Measure, then improve”
  ▲ design becomes more of a formal discipline
◆ Infrastructure
  ▲ design process data collection
  ▲ data mining / visualization / diagnosis
Generic METRICS System Architecture

Inter/Intra-net

Transmitter

wrapper

Tool

Tool

Transmitter

XML

Web Server

DB

Data Mining

Reporting

Java Applets

Metrics Data Warehouse
Benefits of METRICS

- Benefits for design project management
  - Accurate resource prediction at any point in design cycle
  - Accurate project post-mortems

- Benefits for Design Technology R&D
  - Identification of tool sweet spots, key instance parameters
  - Identification of design-process-relevant optimization objectives
  - Feedback from real design activity re tool, parameter usage
  - Real benchmarking via standardized metrics, “no more log files”
Progress: Technology Extrapolation

Recent Developments

- GTX is multi-platform, open-source; two companies using in product (?)
- December 12, 2000 release*: scripting mode, hardwired ORTCs, namespaces, partial rule chain evaluation, vector types, etc.
- Models/studies implemented:
  - cost/yield* (CMU), SOI device/power (Synopsys/Berkeley), RLC interconnect modeling and optimization* (SGI/Synopsys/Berkeley/Sun), routability and layer assignment* (Ghent), manufacturing variability* (Michigan/Berkeley)
- GENESYS, RIPE source code translation into GTX

Near-Term Futures

- Functionality: annotations, “intelligence”, direct Roadmap support
- Calibrations of manufacturing technology (Maly, Strojwas)
- GTX models/studies: RLC interconnect noise/delay (Hu, King, Sylvester), clock dist, device density, DRAM/logic implementation tradeoffs* (Dai), ...
- “Living Roadmap”: GTX = repository for ITRS-2001 material in ORTC, Design, System Drivers chapters
Cost Model - Status

- Two implementations of the cost model:
  - Excel spreadsheet based model
  - GTX based model

- Excel implementation is capable of modeling a multi-product/multi-recipe factory

- Tuned to 0.25 micron CMOS and DRAM processes

- URL: http://www.ece.cmu.edu/~pkn/cost_model/
  - Model details
  - User manual
  - Excel spreadsheets with 0.25 micron process data
Cost Model - Features

- Single product or multi-product/multi-recipe can be modeled
  - 0.25 micron CMOS and/or DRAM processes

- The number of metal layers for each product is variable
  - to study the impact of number of metal layers on cost

- A capacity planning tool is embedded in the model
  - the number of pieces of equipment in a cluster of tools for a process type is calculated for a specified volume.

- The impact of under-utilization of a factory on cost can be estimated
  - the factory can be designed for one volume and cost can be estimated for another value of volume less than equal to the designed-for volume.
Progress: CAD-IP Reuse

◆ Recent Developments*: 16 Bookshelf slots

▲ recent open-source release (MIT license) (since June 2000):

▼ UCLA PDTools (FMPart, MLPart, Capo fixed-die standard-cell placer + support libs)

◆ Capo > 350 downloads (>150 at openeda.org), running at IBM, Intel, Cadence, Sun, Bull, Ammocore, PixelDevices, GeoCast etc. (others like Philips run LEF/DEF based flows around Capo executable); basis of commercial tools; platform for recent academic improvements

▼ UCLA/Ultima bounded-skew clock routing

▼ Rochester/Pitt useful-skew clock design, Binghamton global router

▼ UCSC block packing*, Michigan timing-driven placement, ...

◆ Near-Term Futures

▲ culture change: open-source is the bar for academic reporting, communication

▼ leverage OpenEDA.org, ToolWire, ...

▼ GSRC-supported ↔ open-source in the Bookshelf

▲ interoperability within Bookshelf

▼ data model (e.g., based on DAPIC; promote within academic research community)

▼ vertical benchmarks (data/evaluation, flow research) (Schmit)

▼ more (industry) open-source “Foundation CAD-IP”

▲ better evaluation mechanisms for Bookshelf codes, portable behind firewalls
Floorplanning Slot in Bookshelf

MCNC benchmarks in new GSRC data format

I. Introduction
II. Floorplanning formats (1 blocks, 2 spatial/const)
III. GSRC Floorplan Benchmarks
IV. MCNC Floorplan Benchmarks
V. Floorplanner

I. Introduction and overview

Floorplanning (Block packing) is an essential step in the hierarchical physical design of deep sub-micron VLSI circuits. It is the problem of placing a set of blocks (sub-circuits) without overlap on a layout surface to meet a set of design goals and constraints.
Floorplanning Slot in Bookshelf

New GSRC floorplan benchmarks in 4 levels

Macro GSRC T2 Fabric: Bookshelf

Floorplanning Slot

Work in progress! Last updated: Wed Dec 2, 2000

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I. Introduction
II. Floorplanning formats (1 blocks \texttt{cell}, 2 spatial\texttt{connect})
III. GSRC Floorplan Benchmarks \texttt{cell}
IV. MCNC Floorplan Benchmarks \texttt{cell}
V. Flopplanner

I. Introduction and overview

Floorplanning (Block packing) is an essential step in the hierarchical physical design of sub-micron VLSI circuits. It is the problem of placing a set of blocks (sub-circuits) without overlap on a layout surface to meet a set of design goals and constraints:

- Level I: Hard Rectangle Blocks
- Level II: (Hard + Soft) Rectangle Blocks
- Level III: Hard (Rectangle + Rectilinear) Blocks
- Level IV: (Hard + Soft) (Rectangle + Rectilinear) Blocks

GSRC Floorplan Benchmark Suite

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</table>
Floorplanning Slot in Bookshelf

Example: Level IV
**Recent Developments** (http://vlsicad.cs.ucla.edu/GSRC/METRICS)

- **Industry involvements**
  - proposed standard METRICS naming: generic, tool-specific; flow and process-level metrics
  - open-source middleware for web, database interface
  - Electronic Design Processes Workshop involvement in 2001; greater focus on metrics in ITRS-2001 Design chapter
  - METRICS infrastructure installed and running at Intel, Cadence
  - synthesis metrics developed in partnership with ToolWire
  - entry via regression suites, ASPs: Verilog simulation, logic synthesis, placement, routing, clock distribution, ...

- **Detailed studies using METRICS platform**: wireload models in layout-driven synthesis flows*, routability metrics, timing-driven placement, ...

**Near-Term Futures**

- close eye on standardization (e.g., w.r.t. ToolWire, Synchronicity, Numetrics)
- improved visualization, data mining, process optimization
Summary: Improved Design Technology Productivity

- This Theme promotes mature, coopetitive cultures and shared, open infrastructures that lead to improved creation of design technology.

- Improved vision and design technology planning ("specify"): 
  - What will the design problem look like? What do we need to solve?
  - Answer: Calibration of Manufacturing Technology, and Technology Extrapolation (GTX)

- Improved execution ("develop"): 
  - How can we quickly develop the right design technology (TTM)?
  - Answer: CAD-IP Reuse (Bookshelf)

- Improved measurement ("measure and improve"): 
  - Did we solve the problem (QOR)? Did the design process improve? Did we increase the envelope of achievable design?
  - Answer: Design Process Instrumentation, Optimization (METRICS)