

Overview of IFC Tasks V and VI



- Robert Geer (20 min): Task V Materials and Processing:
Overview and Highlights
- Krishna Saraswat (30 min): 3D ICs: Performance Analysis
and Technology
- Timothy Cale (15 min): Microstructure Formation and Evolution
- Bill Harris (15 min): Metrology Efforts at UAlbany
- Andrew Kahng (10 min): **Wrapup: Impact on Design
and Interactions with GSRC**



End Goal: Technology Extrapolation

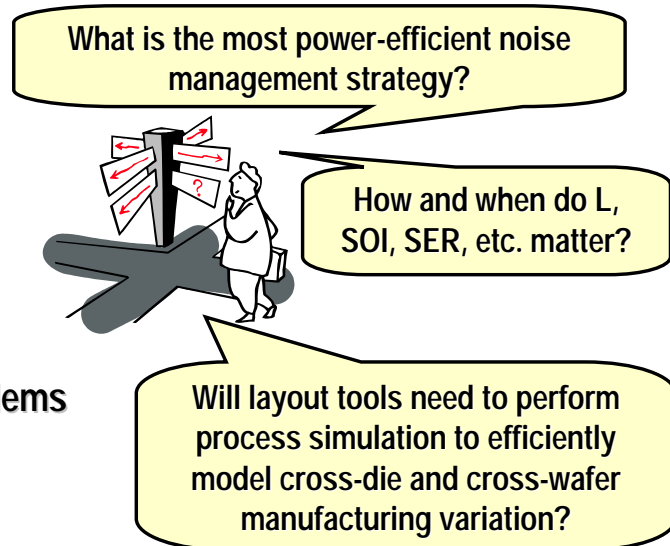


◆ Impact of

- ◆ design technology
- ◆ process technology

◆ Impact on

- ◆ achievable design
- ◆ associated design problems



◆ Sets the requirements for CAD tools and methodologies

◆ Roadmaps: familiar and influential example

Questions and Ideals



◆ Questions

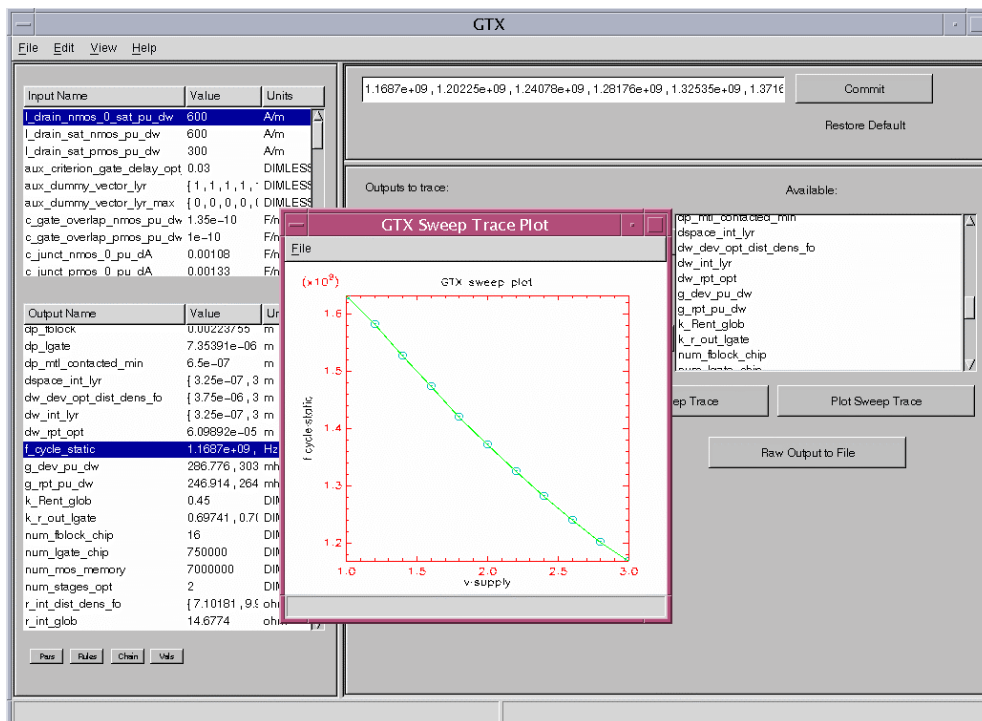
- How do we **assess**, compare, sanity-check modeling choices?
- How do we **reuse** and **extend** models to encompass new technology, new concerns w.r.t. achievable design?

◆ Ideals

- Flexibility
 - ◆ interactive definitions, manipulation of parameters, relations, studies, ...
- Quality
 - ◆ continuous improvement via world-wide participation of experts
- Transparency
 - ◆ open-source mechanism, with models visible to user
- Reduce redundant effort
 - ◆ standard framework; adoptable, extensible, maintainable

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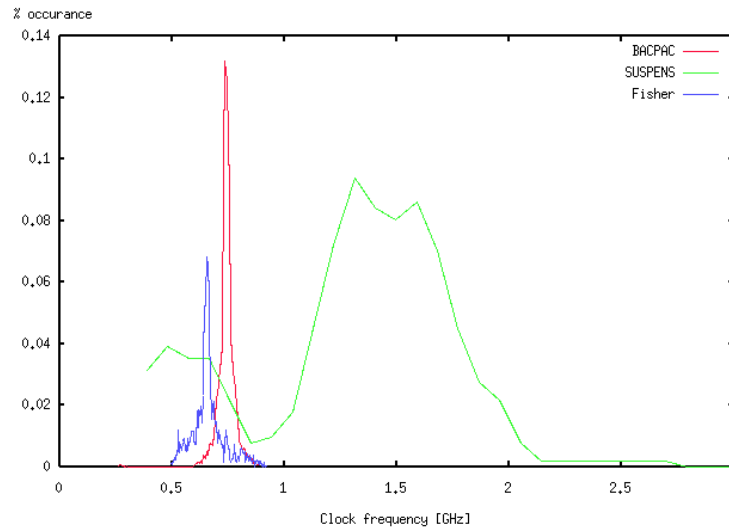
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Parameter Sensitivity



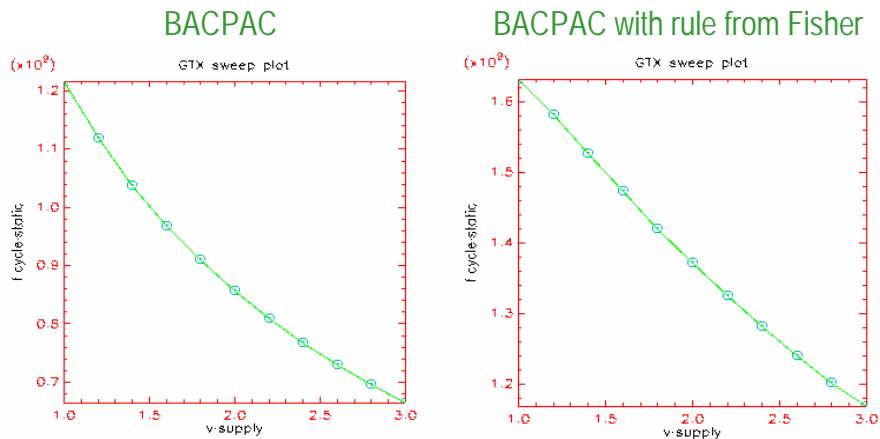
- ◆ Change parameter values and observe resulting difference in outputs



Model Sensitivity



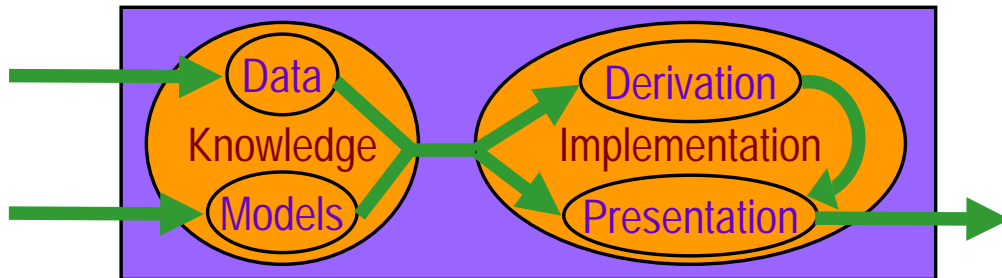
- ◆ Replace rule in a model's rule chain by another model's rule and observe the difference in outputs



GTX: GSRC Technology Extrapolation System



- ◆ GTX is a **framework** for technology extrapolation



- ◆ Flexibility, quality, transparency support “living roadmap”
 - ◆ multi-platform
 - ◆ simple path to capturing expert knowledge: ASCII rules/params
 - ◆ supports optimization / external executables / internal code rules

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GTX Status



- ◆ **Availability**
 - ◆ Cycle-time models (SUSPENS + Takahashi, BACPAC, Fisher) and interconnect tuning studies
 - ◆ Main modules (clock/power, device/power, global interconnect, ...)
 - ◆ Solaris, Windows, Linux platforms
- ◆ **Extensions**
 - ◆ Annotations, namespaces (as in C++), iteration
- ◆ **Implementations within GTX**
 - ◆ Synopsys/UCB: device/power, SOI device, (reliability)
 - ◆ others: via impact, cost/yield, architecture, inductance, ...

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Tasks V, VI : Impact on Design, and Interactions

- ◆ **Implications of 3D IC technology on circuits, architectures**
 - ◆ k-layer and 3D
 - ◆ buffer insertion, critical-path layout, uP floorplan (cache), AMS, ...
 - ◆ general questions of embedding strategy and embeddability
- ◆ **New conductors and insulators**
 - ◆ behind and beyond rho, k, variability
 - ◆ PPPP models
 - ◆ expanded materials set, hybridizations/integrations
 - ◆ new criteria, issues
- ◆ **Impact on other axes of achievable design**
 - ◆ power, manufacturing cost/yield, ...
- ◆ **Encapsulation within GTX framework ?**