Foundations for **Understanding Achievable Design**:  
Ground Truths, the Bookshelf, and Metrics

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**Theme Evolved From Thrust**

- **1997-1998**: Rebuild the RTL Foundation  
  - predictors and predictability  
  - “unifications” of logic-layout, layout-manufacturing, temporal-physical, synthesis-analysis, ...
- **November 1998**: “Design as Optimization”
- **November 1998**: “Ground Truths”
- **February 1999**: “Bookshelf” and Fabrics projects/clustering
- **April 1999**: “Measure, Then Improve” (aka “Metrics”)
- **June 1999**: Foundations for **Understanding Achievable Design**:  
  Ground Truths, the Bookshelf, and Metrics
Precepts

- System design is based on:
  - design optimization
  - prediction
- GSRC must prove:
  - real collaboration ("combine strengths"); whole > sum of parts
  - critical mass and influence to create community-wide culture change
  - its effect on the real-world practice of design and test
- This Theme’s answer:
  - ground truths
  - the bookshelf
  - metrics

1. Ground Truths

- Fundamental facts and data points that anchor the process of bounding the achievable envelope of design
  - ground truths must be identified and propagated
- Can be with respect to:
  - manufacturing process, materials, physical phenomena
  - specific CAD optimizations of circuit topology/embedding
  - system architecture and packaging
- Are properly extrapolated via:
  - "inference chains"
  - response surface modeling and parameter optimization
- Drive the EDA community’s vision of future design issues:
  - current distribution, inductance extraction, UDSM testing, …
  - fundamental limits
Example Ground Truths

- What is the maximum possible clock frequency for a given process and die size?
- When does inductance matter?
- What design tradeoffs must be made to maintain reasonable supply currents?
- What is the necessary number of package pins/balls for power/ground distribution?
- At what geometries, supply voltages will domino lose most advantages over static CMOS?
- (recall: what are extreme fabrics? what are limits of existing fabrics?)

Ground Truths Status

- Drawing on RPI, GaTech, Berkeley (KK,CH), Rockwell, ...
- Jason: (models of) BIS/WS-optimized, multi-terminal global interconnects
- Wayne: (models of) block packing to improve bounds on top-level interconnect requirements
- Wojciech: cost modeling, cost implications (2nd half today)
- Issues:
  - software architecture (Java, C++, website)
  - use model (data security, data collection, …)
  - etc.
2. The Bookshelf

- “Inference chains" through function block, Rent parameter, floorplan, etc. levels of system abstraction must have relevant abstractions
  → high-quality models of high-quality heuristic optimizations
- **The Bookshelf**
  - framework to enable shared, community-wide maintenance of state for key pieces of the (CAD algorithms) R&D leading edge
  - remove barriers to entry for algorithm research -- and adoption of algorithm research -- at the leading edge
- **Bookshelf Slot: “key problem for the VLSI CAD field”**
- **Bookshelf = repository for leading-edge innovations -- and their implementations -- for solving this problem**

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The Bookshelf (cont.)

- **For given Bookshelf slot, several basic types of entries**
  - canonical problem definition (e.g., C++ class + supporting packages)
  - reference solver implementations
  - **benchmark data**
  - heuristic evaluation and comparison methodology
  - N.B.: “bookshelf” extends “benchmark” concept to encompass reference implementations and other R&D infrastructure
- **Bookshelf framework allows :**
  - improved effectiveness and impact of heuristic algorithm research in VLSI CAD
  - more rapid communication between research groups
  - more rapid adoption of research advances by industry
  - path to evolvable GSRC implementation flows/methodologies
The Bookshelf Status

* One bookshelf slot (FM partitioning) populated, sent to John Reekie for comments; global cell placement to follow
* Jason: single interconnect topology optimization with BIS/WS degrees of freedom
* Wayne: block placement (area, wirelength, timing driven)
* Build system (archive + config script = portable build system) candidate setup created, sent to John Reekie for comments, iteration
* Bookshelf proposal, software survey distributed
* Backplane
  – baseline implementation flow being sought (mini-flow from above)
  – CHDStd on IBM/Cadence is very promising development
* Issues: mechanisms for propagation through community

3. Metrics

* Design optimization must be founded on
  – an understanding of what should be optimized by which heuristic
  – an understanding of design as a process
* “Metrics” supports original M2 ideal of ”measure, then improve”
  – design becomes less of an art and more of a formal discipline
  – design process optimization enabled through framework of recording, mining, measuring, diagnosing, and then improving
* Infrastructure
  – requires “proactive” initiative from EDA vendors
  – designer and design tools R&D communities: (i) what should be measured, (ii) data mining / visualization / diagnosis infrastructure, (iii) project-specific design process data collection
Metrics Status

- Metrics IP / infrastructure
  - OxSigen LLC
  - data model, API, applet to write out metrics embedded in tools
  - proof of concept: Cadence physical verification project initiated?
  - existing OxSigen scripting wrapped around log files metricizes baseline GSRC implementation flow
- Working on more DPO buy-in from big EDA companies
  - e.g., convince that there is a business case
- Working on pull from big customers = GSRC sponsors

Theme Participation

- Kurt 20%
- Jason 33%
- Wojciech 50%
- Wayne 75-100%
- Andrew 100%
Visualize December

- **Ground truths system, v1.0**
  - arbitrary tradeoff studies, parameter optimizations
  - accurate models of optimization effects in layers between individual wires/devices and system architecture
  - cost modeling
  - understanding of how wrong/correct answers to the above questions can be
- **Bookshelf**
  - well-publicized goals, standards
  - 3-5 slots instantiated with entries from multiple investigators
  - mini-flow built around soft-block packing/global interconnect opt/cell placement
- **Metrics**
  - two of largest EDA vendors have metricized at least one major tool
  - T2 members all run metricized implementation methodology

Collaborative Infrastructure

- **Website with discussion boards, research material upload and linked messaging**
- **Baseline implementation tool flow for flat or two-level hierarchical physical chip implementation**
We understand that it is difficult (perhaps impossible) to obtain a “real, industry” design driver.

Having said this, possible improvements would be:

- Push limits of technology and limits of CAD
- Limits of frequency, power / clock distribution
- uP-like (e.g., lots of cache)
- Complex timing architecture?
- Size: large if possible
  - drive logical partitioning, global interconnect/clock optimization, …
- “Front-to-back” (includes package DOF’s)
- Very important: complete information (all views, all stages)