Transition Aware Global Signaling (TAGS)

- Proposed as an alternative to standard inverter receivers
- Enables a 15mm unbuffered line with a 800MHz global clock, repeater scheme required 3 repeaters to meet same delay requirement.
- Results in up to 26% power savings and more than 50% savings in total device width for driving a long line.
- Very robust in the presence of functional noise at the end of the line.
Active Shields: Signal nets

- Switch shields to help signal propagation and/or improve noise immunity
- For RC lines switch shields in phase with signal net to reduce effective coupling capacitance
- Foot print of fat wire and passively shielded wire kept constant when converted to actively shielded version
- Capacitive loading on previous stage kept constant
- Actively shielded wire resulted in upto 16% and 29% improvement in delay compared to passively shielded and fat wires, respectively.
- Active shielding approach being extended to reduce noise and delay in the presence of inductive effects
- To appear in Great Lakes Symposium on VLSI (GLSVLSI) 2002
Active Shields: Clock nets

- Original “fat” clock net split up
- Clock sensed only on middle net
- Side nets now serve as active shields to reduce Miller capacitance
- Resulted in ~17% and ~20% improvement in delay and rise/fall times, respectively. Power consumption remained constant.
- Approach being extended to include inductive effects. Active shields will have to switch in opposite phase to reduce return path

![Diagram of Active Shields: Clock nets](image)

Improved slope and delay