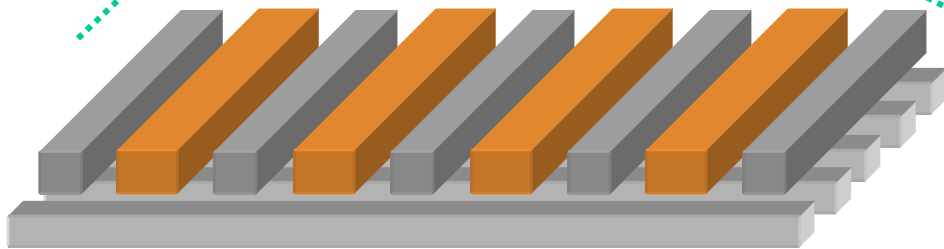
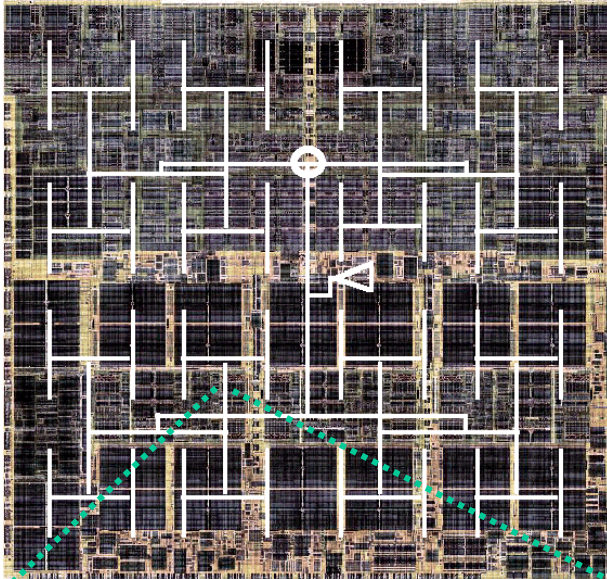


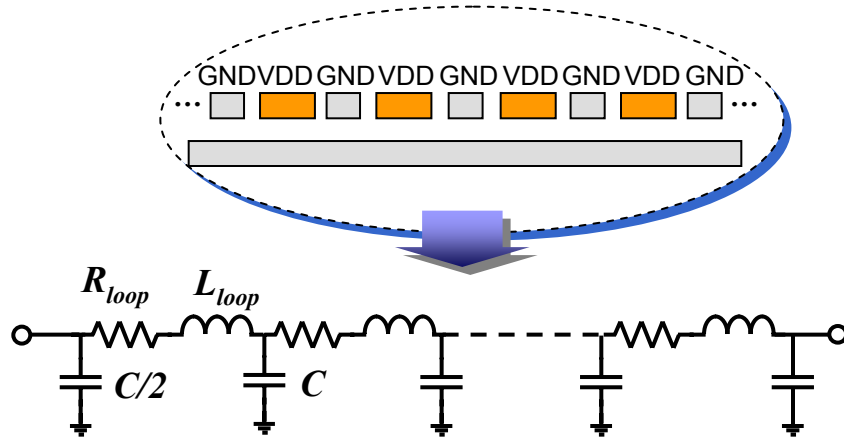
Interconnect modeling for multi-GHz clock network



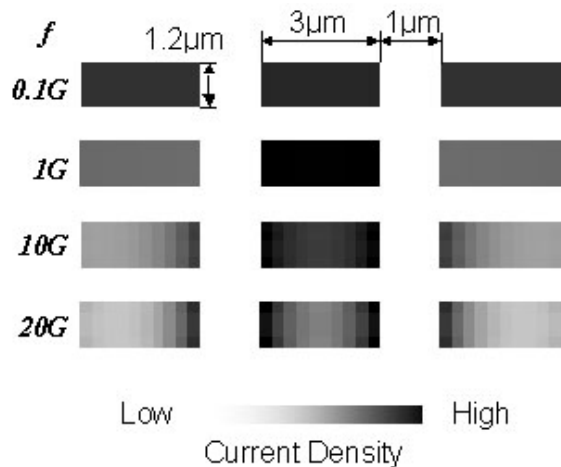
- Special interconnect structure
 - Wires highly optimized with VDD/GND shields
 - Wide lines split into multiple fingers interspersed with shield to suppress inductive ringing
- Efficient models needed for fast optimization and physical design exploration
- High frequency effects including inductance need to be captured for multi-GHz design

Loop-based interconnect model

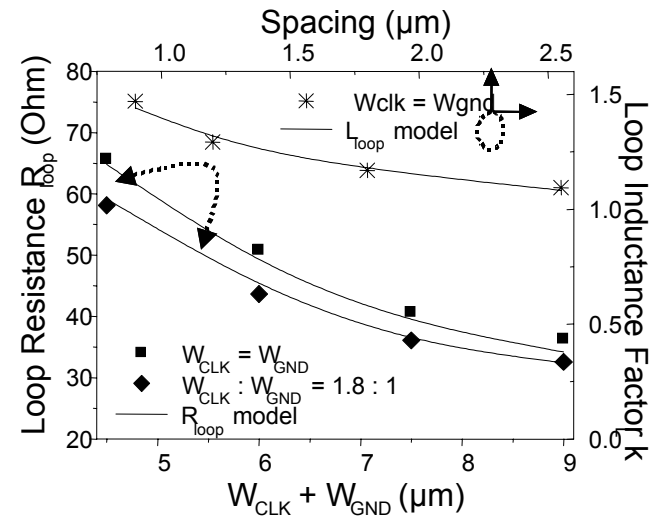
Interconnect Model



Proximity Effects

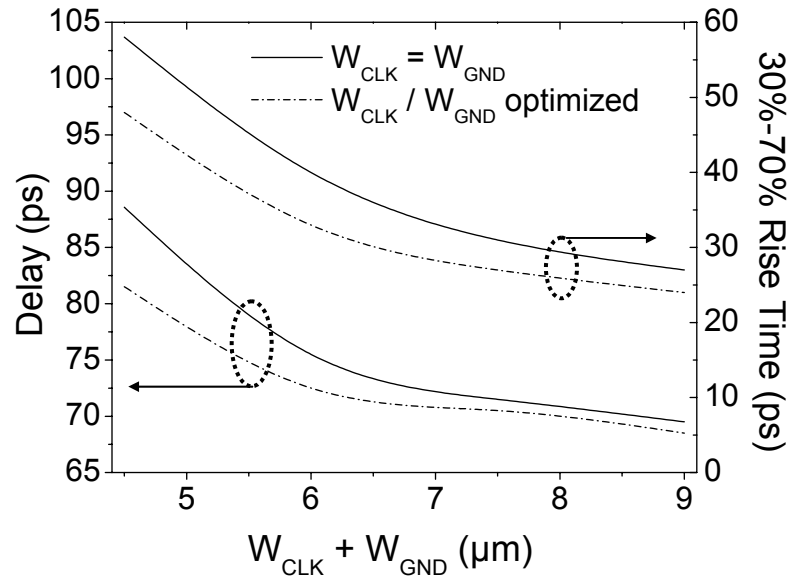


Model Verification



- Entire signal and return loops represented by a single RLC ladder circuit with effective R_{loop} and L_{loop} .
- Loop RL calculated from analytical equations based on geometry and frequency
- Proximity effects are captured

Interconnect Optimization



- Interconnect geometry optimization possible based on developed analytical models
- This methodology greatly reduces simulation complexity at the same time maintains good accuracy
- Details will be presented in CICC'02, May 2002.