

GTX DRAM Model

- ◆ Developed DRAM area/access time model based on conventional asynchronous DRAM architecture (FPM, EDO, etc.)
- ◆ Derive the DRAM area and access time based on architectural parameters (size, IO width, address width, etc.) and technological parameters (feature size, transistor size, cell capacitance, etc.)
- ◆ Focus on the DRAM core area efficiency and critical datapath.
- ◆ Enable the designers to analyze the DRAM cost and performance without actual physical implementation.
- ◆ Need DRAM technology information and detailed circuit architecture to further verify the model and tune the parameters.



Next Step

- ◆ Convert DRAM access time model to GTX format.
- ◆ Collect data for DRAM technology and circuitry.
- ◆ Develop DRAM power model and cost model (from area model).
- ◆ Verify the DRAM access time model with available industrial data; develop a set of parameters for current DRAM technologies.
- ◆ Develop model for SiP power/ground and clock distribution, evaluate SiP performance against SoC and off-chip implementations.
- ◆ Compare the area/delay/power of embedded DRAM and DRAM for System-in-a-Package (SiP), as well as the conventional DRAM implementation.

