

**SITS**

**Single Interconnect Tree Synthesis  
slot status**

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# Status

- Rev 1.2 of file formats
- Three solvers posted + TRIO
  - P-Tree (Linux & Solaris executable)
  - S-Tree (Linux & Solaris executable)
  - Static topology optimizer (source code)
- GUI versions in progress (PostScript output available)
- Sample instances available
- Relevant papers posted

# Since last meeting

- Fundamental Technology slot under revision
  - New format for Target Routing Graph (in progress)
- New solver posted
  - Static topology optimizer (source code)
- Developed new solver
  - SP-Tree (to be posted soon)

# Since last meeting (cont.)

- Development of GUI versions postponed
  - Instead, solvers output solutions in both GSRC format and PostScript (see last slide)
- Relevant papers posted (P-Tree, S-Tree, SP-Tree)

# To Do List

- Synchronize data formats with Fundamental Technology slot
- Post two more solvers
  - Soft edges topology optimizer
  - SP-Tree
- GUI versions of all solvers
- Industrial benchmark instances?
- Post additional source codes

# Example of new output

