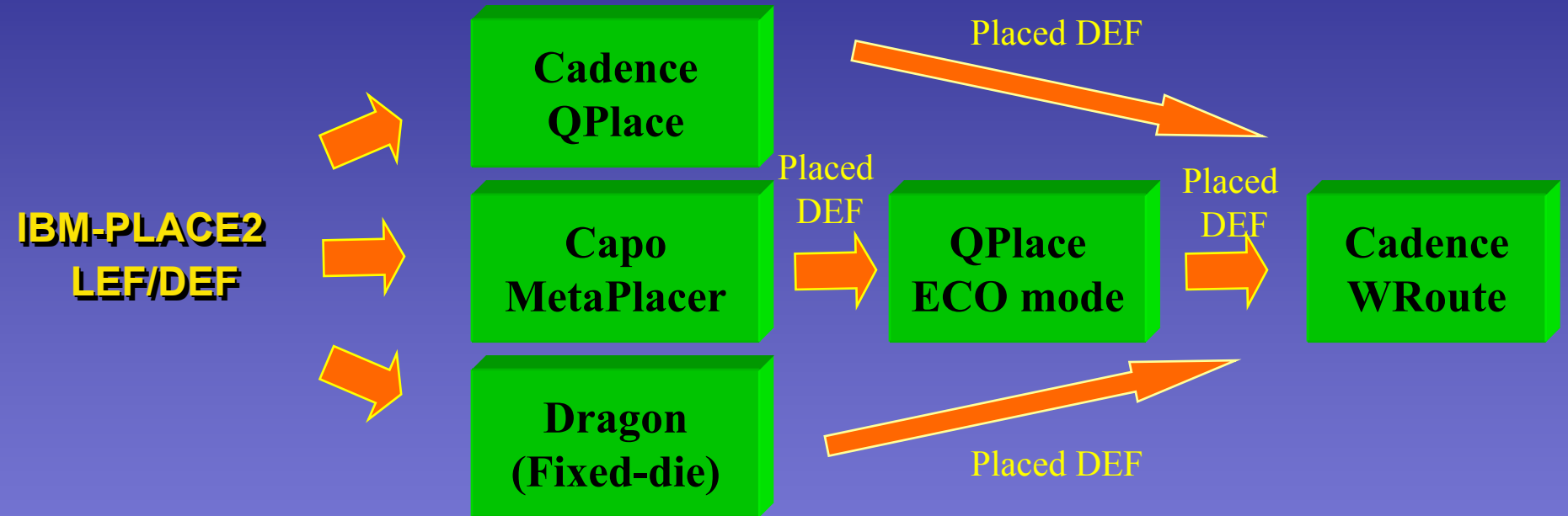


Experimental Setup



Benchmarks (IBM-PLACE 2.0)

- Converted from ISPD98 partitioning suite, floorplanned by Cadence Silicon Ensemble
- New features for IBM-PLACE 2.0:
 - LEF/DEF and GSRC bookshelf format
 - Cell sizes are similar with the standard-cells in TSMC 0.18um library (from Artisan Inc.)
 - Aspect ratio 1.0 (arbitrary number of rows)
 - No space between rows
 - Exact pin locations (not center-of-cell)
 - Over-the-cell routing with 4 or 5 routing layers
 - Predefined core size with white space 5%-15%
 - Each circuit corresponds to an easy and a hard instance
- Limitations
 - No clock/power/ground signals
 - No pin input/output information
 - No I/O pads connections

Place/Route Flow

- QPlace
 - Congestion-driven (default) mode
- Capo/MetaPlacer
 - Default mode
 - A post-placement step (QPlace ECO mode) is required to correct small displacement problems
- Dragon
 - Fixed-die mode with white space allocation
- WRoute
 - Both global and detailed routing
 - Reporting final wirelength, number of violations and vias, routing time.
 - Automatically stopping if the placement is unroutable

Details

- Input files
 - QPlace: configuration file, LEF, floorplanned DEF
 - Capo/MetaPlace: auxiliary file, LEF, floorplanned DEF
 - Dragon: configuration file, LEF, floorplanned DEF
 - ECO for Capo/MetaPlace: configuration file, LEF, floorplanned and placed DEF
 - WRoute: configuration file, LEF, floorplanned and placed DEF
- Routing result
 - Successful without violation
 - With lots of iterations and a small number of violations
 - Failed because of too many violations
- GSRC bookshelf format
 - Dragon website will provide the benchmarks for both LEF/DEF and bookshelf format, and the converter from placed bookshelf files to DEF files <http://er.cs.ucla.edu/Dragon>