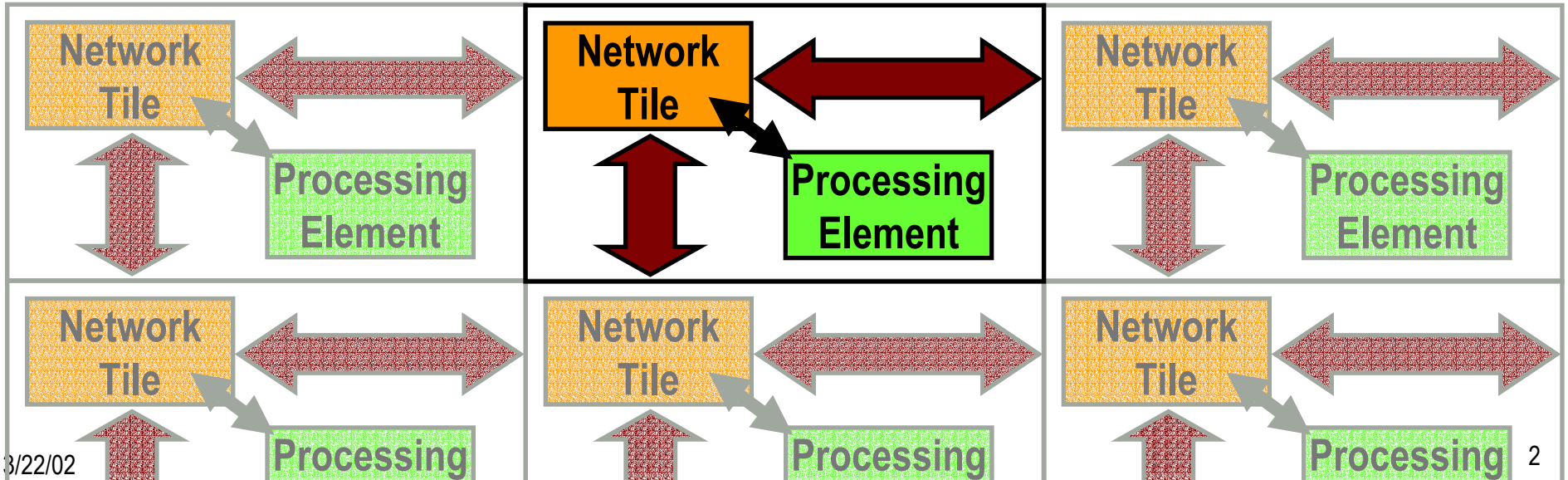
Benchmark Update

- Carnegie Cell Library: “Free to all who Enter”
  - Need to build scaling model of standard cell library
  - Based on our open 0.35 micron library (real extracted data)
  - This semester: basic standard cells
  - This summer: memories
- Timing Models
  - Actual timing probably is not as important as variations
  - Simple 1-order models of speed and variations

Circuit Benchmarks

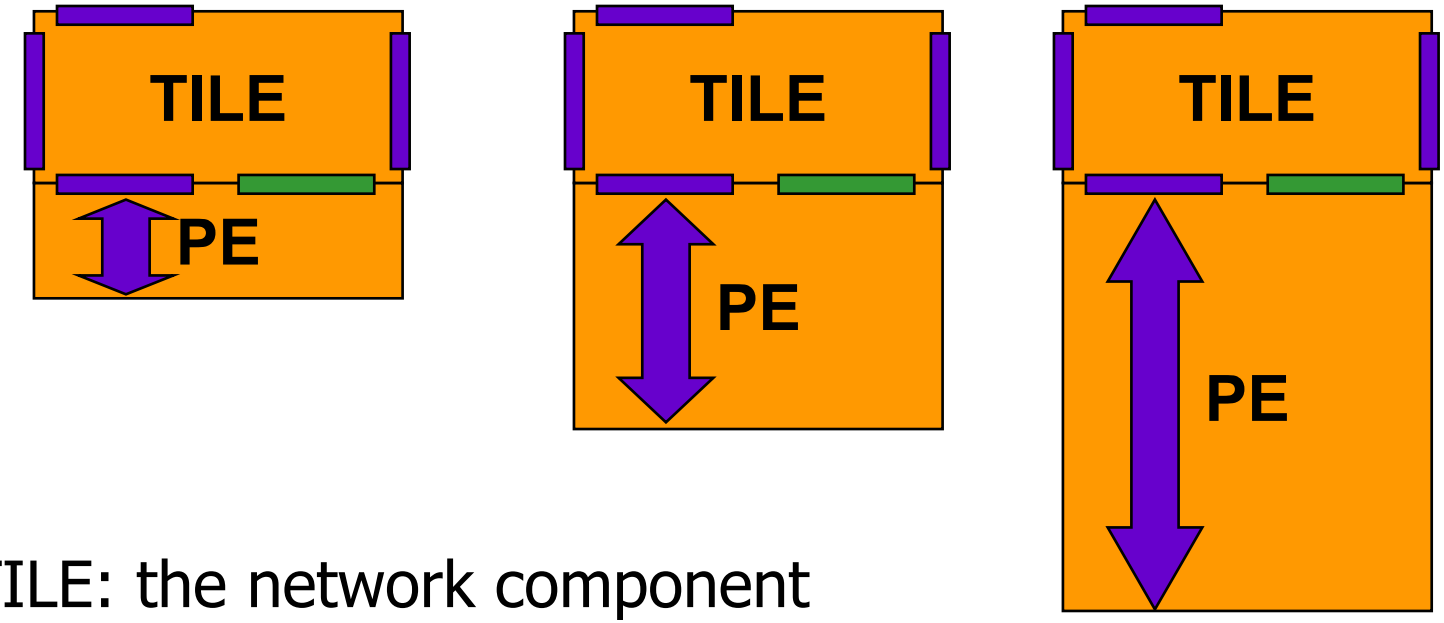
- **New vertical benchmarks:**
  - All designed to comply with common network interface
  - Interoperability, portability for IP blocks
  - Why is this interesting/useful for benchmarks?
    - IOs and other system-level issues make it hard to compare benchmarks
  - Also good for education



New Circuit Bencmarks

- The Network Tile: for streaming applications
- The Processing Elements:
  - Morphable Floating Point Multiplier:
    - FP mult and vector add, integer multiply and integer MAC and shift
  - Morphable Floating Point Adder:
    - FP add and integer add and shift
  - Programmable Integer ALU
  - Programmable FIR filter
  - SIMD Adder (with funky completion logic)
- All about 20-100k gates each
  - Can be combined into systems of arbitrary size
  - Network limits effective Rent's Exponent
  - *Actually Network connectivity would determine Rent Exponent
    - Currently planning 2-D network, creating Rent Exponent of 0.5

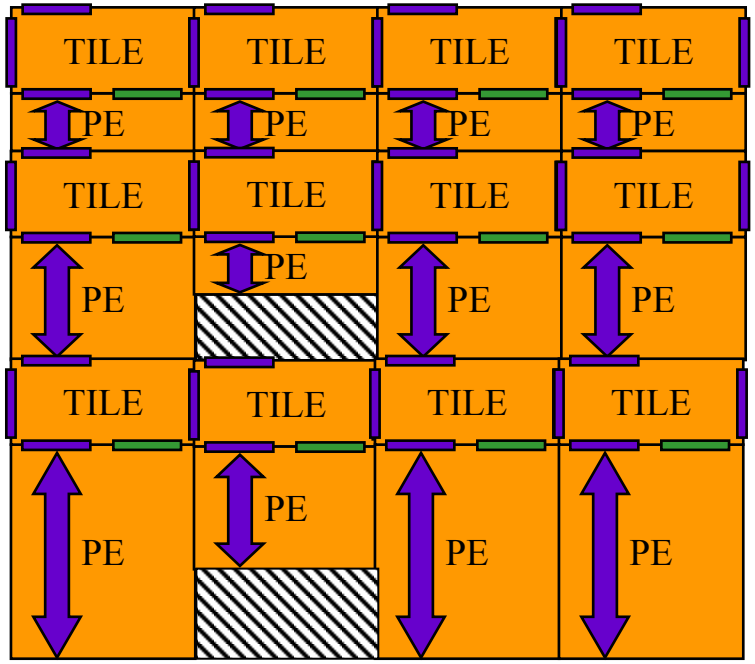
Dynamic Network Tiles



TILE: the network component

PE: the component at this node in the network

Dynamic Network System



Reference Clock distribution through network

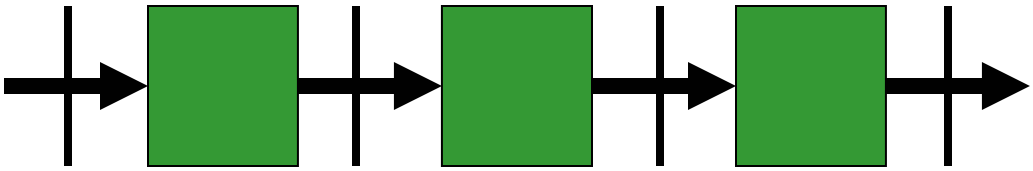
Each tile generates own clock

Interface decoupled via FIFOs

New Placement Problem: space utilization vs. distance

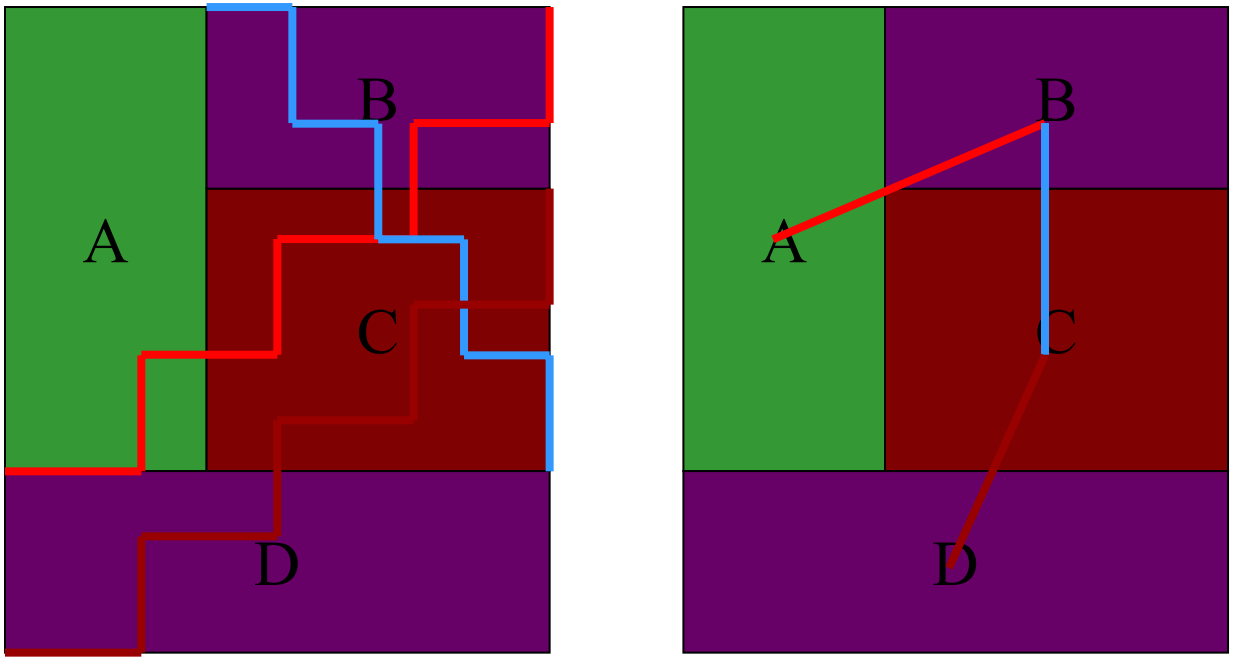
Target Architecture:

Pipelined Arrays



- Limited Feedback
- Long/short wires predictable
- Clock Skew
- Important Application Domain

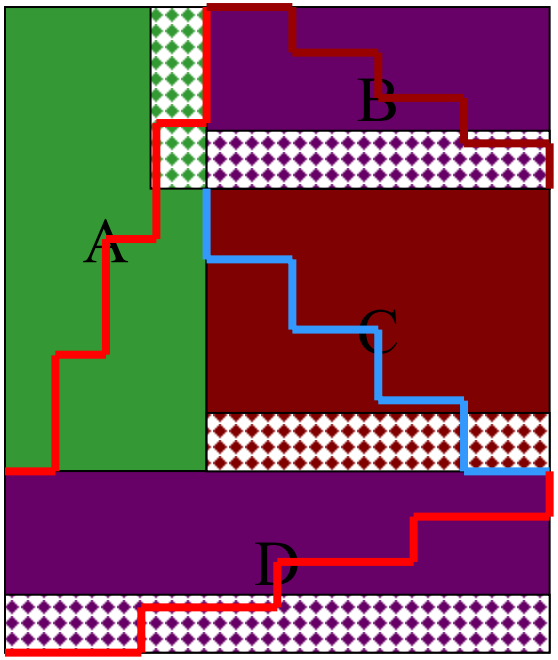
Classic Wire Length Models

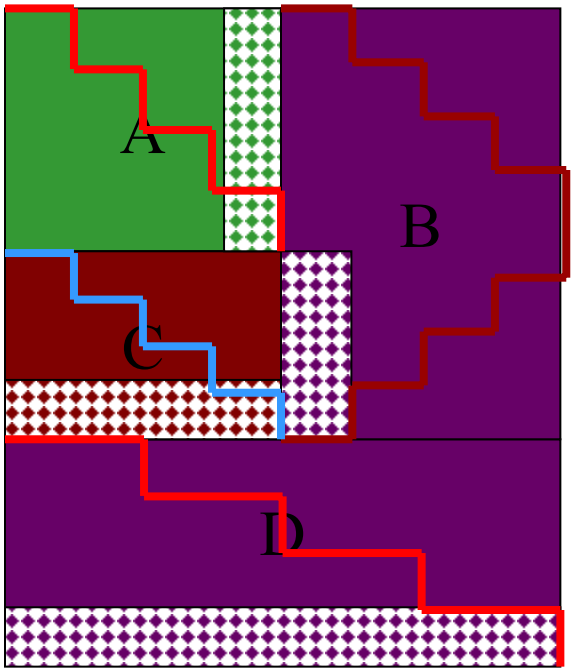


Wire Path Length

- Every block is a pipeline stage
- Impossible to determine every wire length from floorplan blocks
- Wire Path Length (WPL) measures the distance between consecutive registers

Wire Path Length

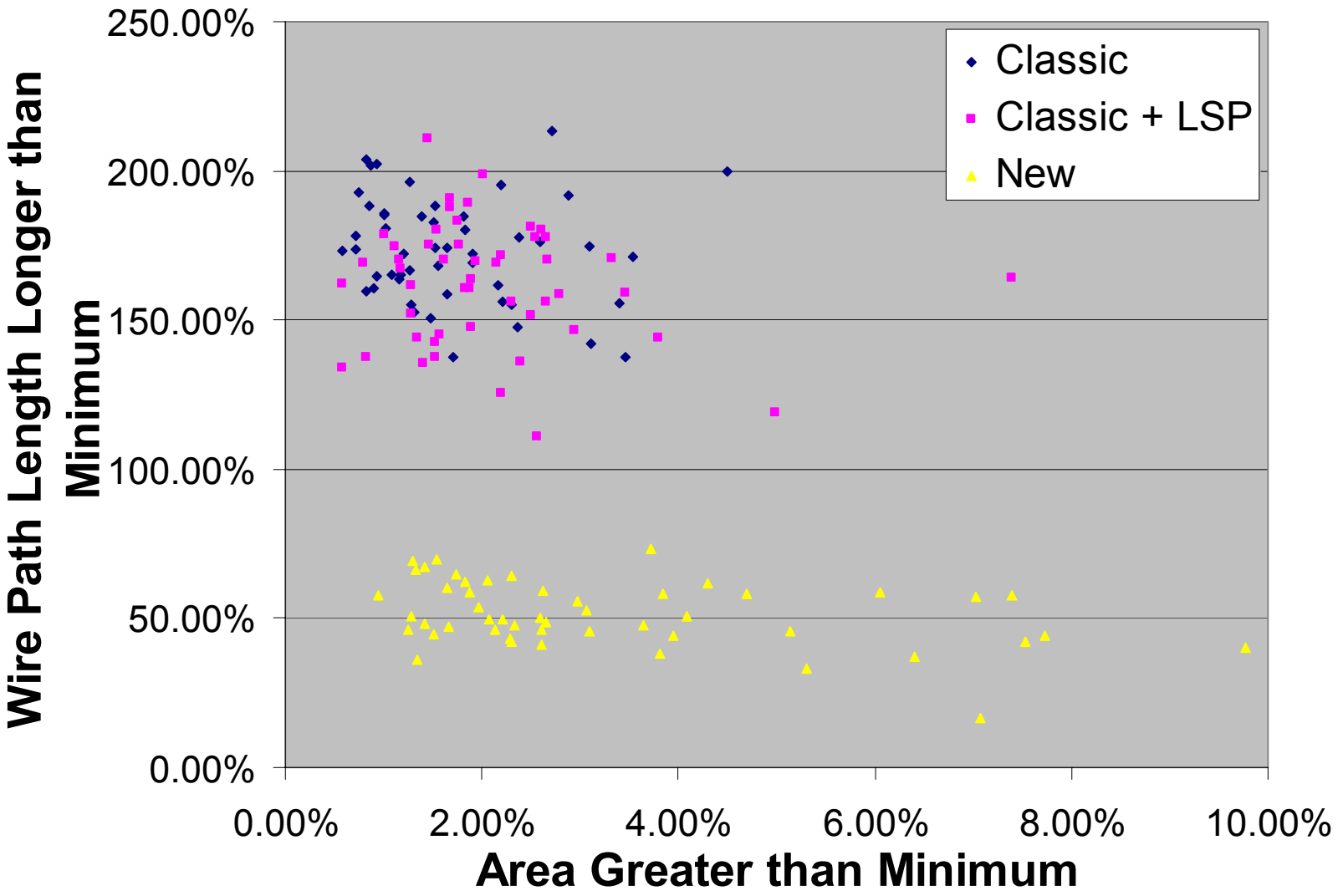




Results Key

- Classic
  - Different random starting position every time
  - Classic Move Set - Swap
- Classic + LSP
  - Same legal starting position every time
  - Classic Move Set - Swap
- New
  - Same legal starting position every time
  - New Move Set - Insert/Delete

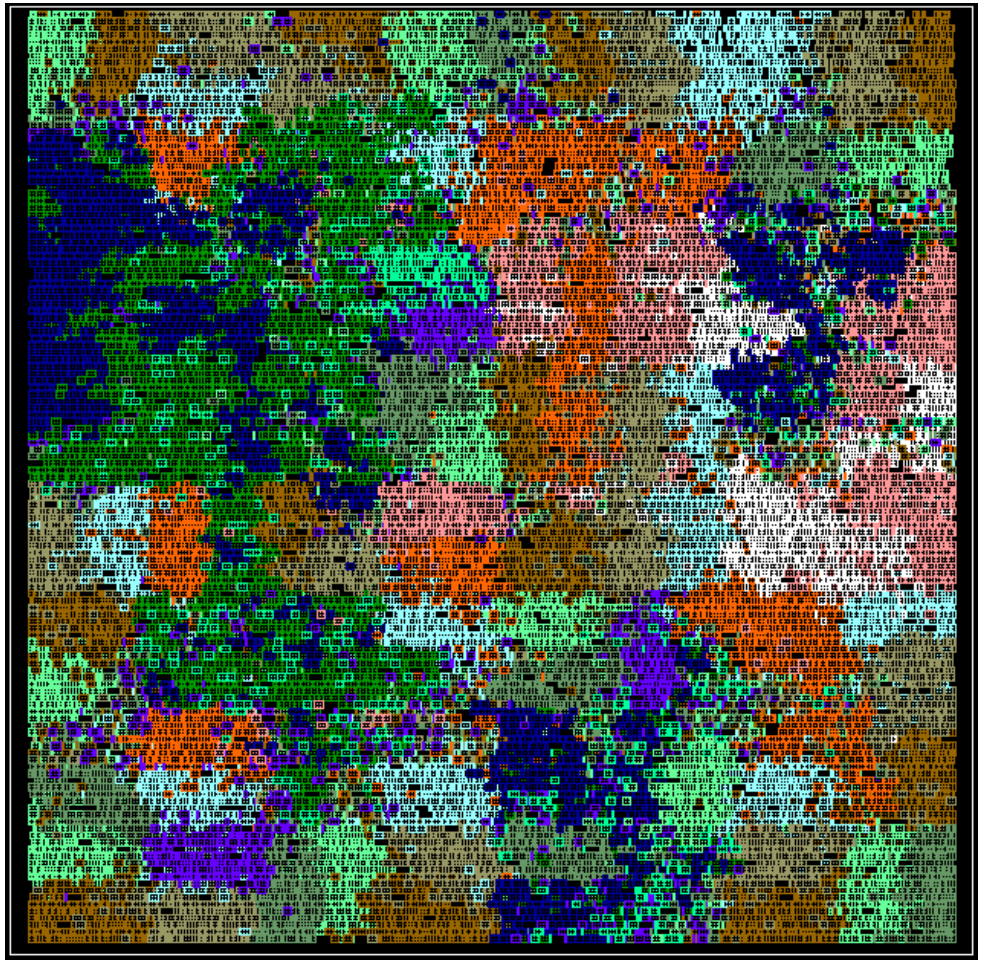
IDEA 60 Block Design



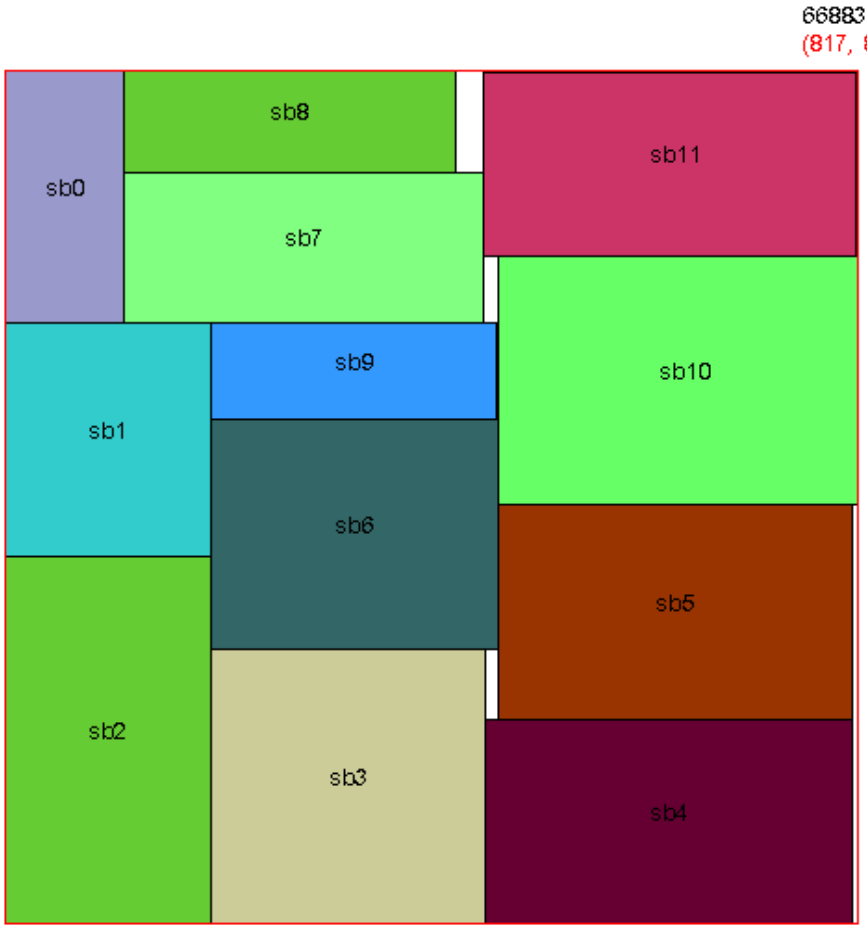
1-D DCT

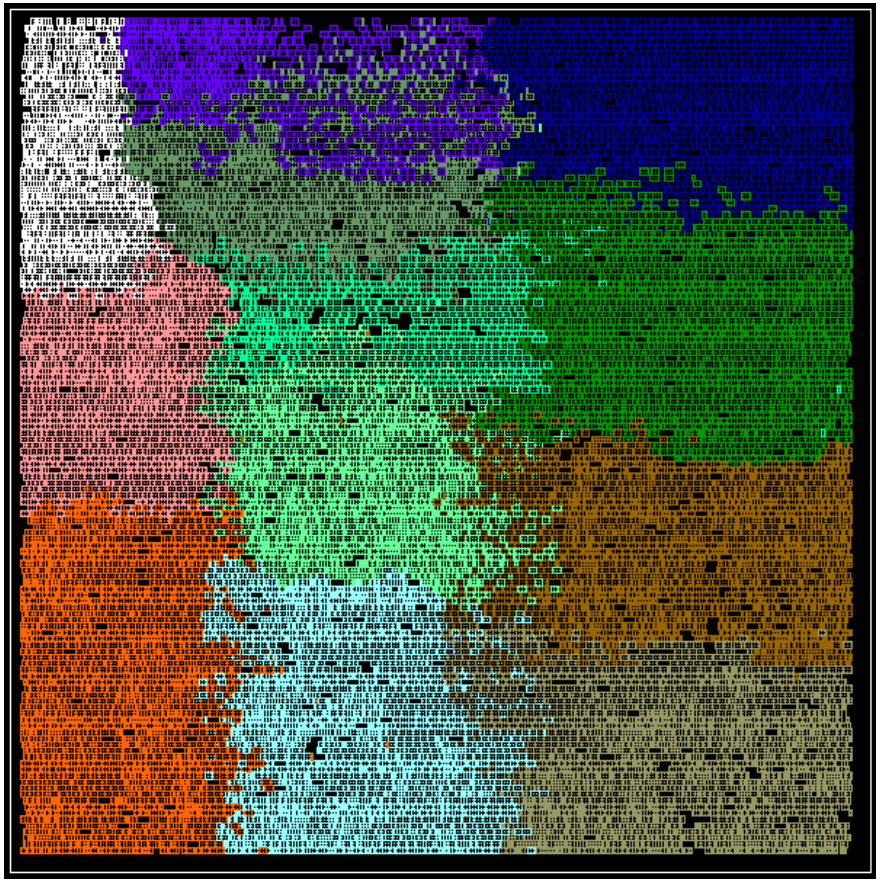
- 12 Pipeline Stages
- Synthesis Speed - 2.25 ns.
- Synthesis Area - 668,323 μm^2

Unfloorplanned



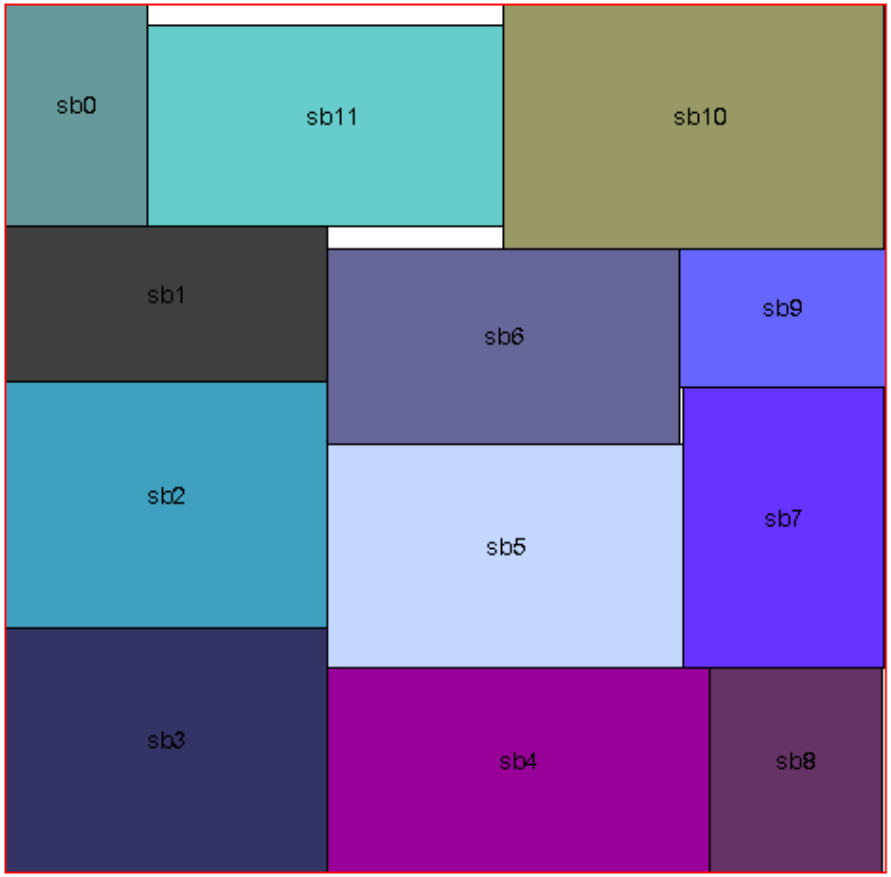
Classic

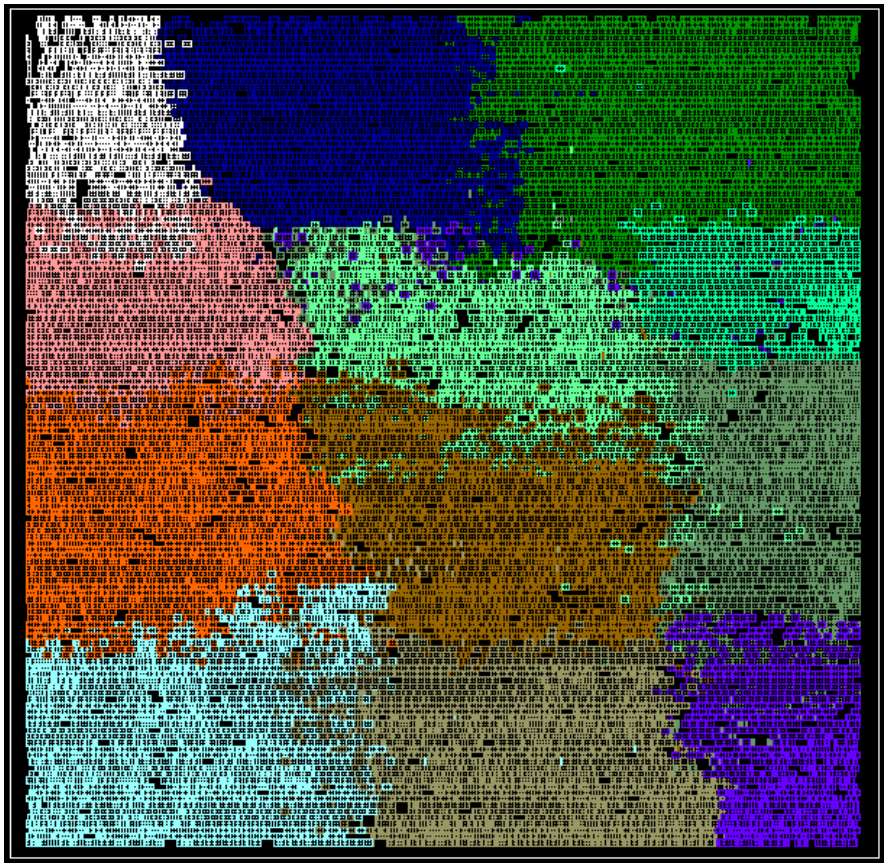

668830
(817, 817)
sb0
sb8
sb11
sb7
sb9
sb10
sb1
sb6
sb5
sb2
sb3
sb4



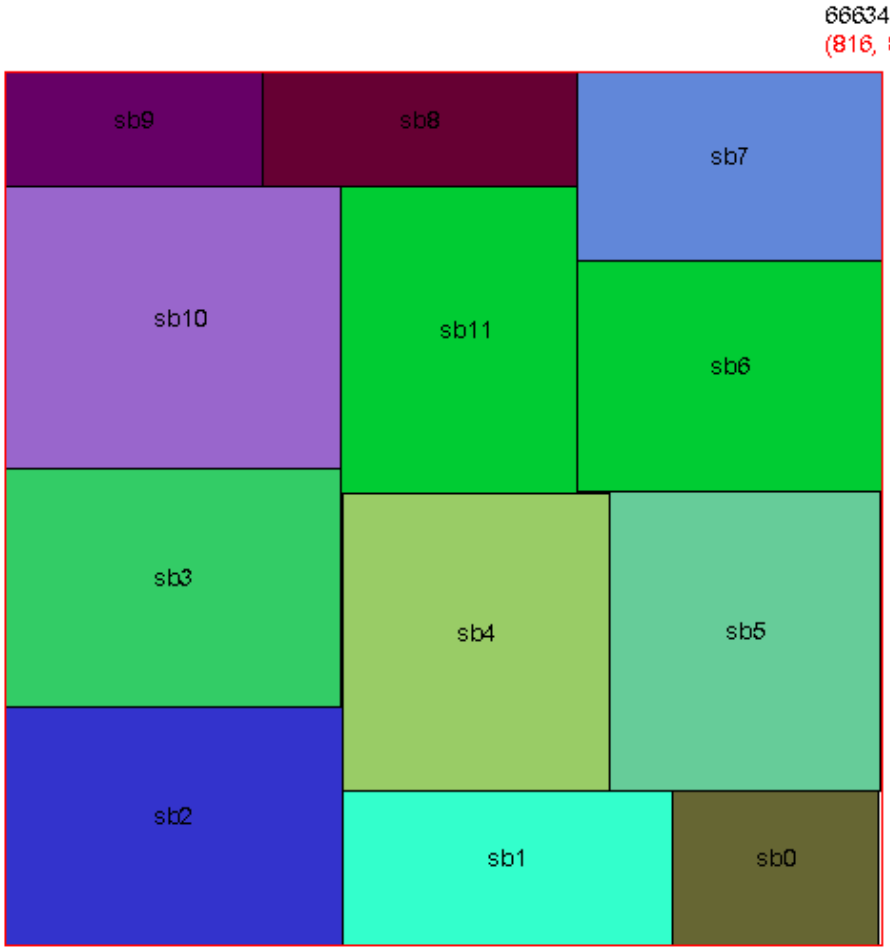
Classic + LSP

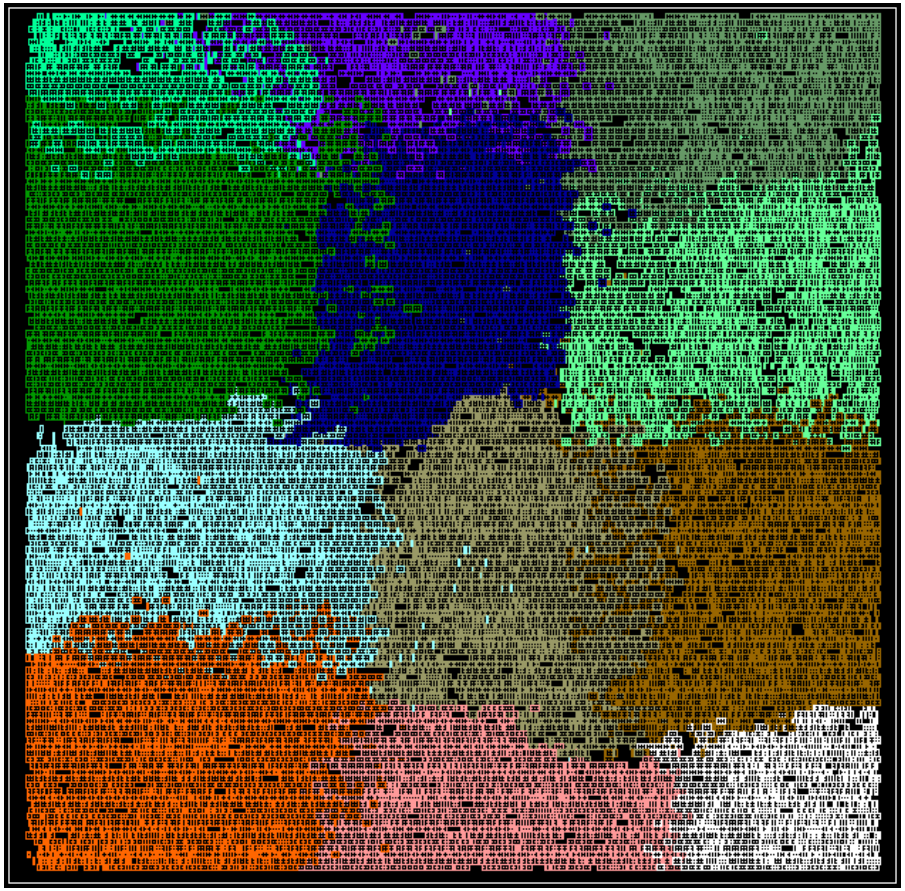
673338
(825, 815)





New


666340
(816, 815)
sb9
sb8
sb7
sb10
sb11
sb6
sb3
sb4
sb5
sb2
sb1
sb0



Results

	Dead Space	WPL	DRCs	Speed	Avg. Cong.	Max Cong.
No Floor	X	X	0	2.50	0.35	0.98
Classic	0.97%	6.15	850	2.40	0.60	1.32
Classic + LSP	1.63%	5.88	138	2.44	0.57	1.31
New	0.09%	5.76	12	2.37	0.54	1.19