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Scope: Increased manufacturing variability in leading-edge process technologies requires new paradigms and solution technologies for yield optimization. SoC manufacturability and yield entails design-specific optimization of the manufacturing, and thus enhanced communications across the design-manufacturing interface. A wide range of Design-for-Manufacturability (DFM) and Design-for-Yield (DFY) methodologies and tools have been proposed in recent years. Some of these tools are leveraged during back-end design, others are applied post-GDSII (just before manufacturing handoff), and still others are applied post-design, from reticle enhancement and lithography through wafer sort, packaging, final test and failure analysis. DFM and DFY can dramatically impact the business performance of chip manufacturers. It can also significantly affect age-old chip design flows. Using DFM and DFY solutions is an investment, and choosing the most cost effective one(s) requires careful analysis of integration and schedule overheads, versus quantified benefits. This workshop analyzes this key trend and its challenges, and provides an opportunity to discuss a range of DFM and DFY solutions for today's SoC designs.

Representative topics include, but are not limited to:

- *Electrical, Design-Driven DFM*
- *Built-in Repair Analysis and Self-Repair*
- *Random Defectivity and Critical Area*
- *Adaptive Design Techniques in DFM/DFY*
- *Embedded Test and Diagnosis*
- *Infrastructure IP*
- *OPC and RET*
- *Analog and mixed-signal DFM*
- *Process Monitoring IP*
- *Statistical Design*
- *Test-based Yield Learning*
- *Variability-aware Design*
- *Yield Enhancement IP*
- *Yield Management*

Author information

To present at the Workshop, authors are invited to submit paper proposals. The proposals may be extended abstracts (500 words) or full papers. Each submission should include: title, full name and affiliation of all authors, a short abstract of 50 words, and keywords. Also, identify a contact author and include a complete correspondence address, phone number, fax number, and e-mail address.

Submit a copy of your paper proposal by Postscript, or PDF, via E-mail. Proposals for panel discussions are also invited. Submissions are due no later than **August 31, 2007**.

Submit your paper proposal to:

Andrew B. Kahng, UC San Diego E-mail: abk@ucsd.edu Tel: +1-858-822-4884

Authors will be notified of the disposition of their papers by **September 18th, 2007**.

Authors of accepted papers to submit an illustrated text by **October 3rd, 2007** for inclusion in the Workshop Notes, which will be provided to the attendees.

Special Issue: The best contributions of DFM&Y 2007 will appear in a Special Issue of JETTA (the Journal of Electronic Testing: Theory and Applications)

DFM&Y 2007 is sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and in cooperation with the IEEE Council on Electronic Design Automation (CEDA). For more information on DFM&Y 2007, visit the workshop website at:

<http://www.unipi.gr/dfmy>

